The DIALOG Chip in the Front-End Electronics of the LHCb Muon Detector

Sandro Cadeddu, Caterina Deplano and Adriano Lai, *Member, IEEE*

***Abstract*— We present a custom integrated circuit, named DIALOG, which is a fundamental building block in the front-end architecture of the LHCb Muon detector. DIALOG is realized in IBM 0.25 um technology, using radiation hardening layout techniques. DIALOG integrates important tools for detector time alignment procedures and time alignment monitoring on the front-end system. In particular, it integrates 16 programmable delays, which can be regulated in steps of 1 ns. Many other features, necessary for the Muon trigger operation and for a safe front-end monitoring are integrated: DIALOG generates the information used by the trigger as a combination of its 16 inputs from the Amplifier-Shaper-Discriminator (ASD) chips, it generates the thresholds of the ASD, it monitors the rate of all its input channels. We describe the circuit architecture, its internal blocks and its main modes of operation.**

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I. Introduction

THE LHCb experiment [1], currently under construction at the CERN (European Center for Nuclear Research) LHC (Large Hadron Collider), will study the CP violation and B mesons rare decays. The LHCb Muon Detector is especially important in the first LHCb trigger level, the level zero trigger (L0) in LHCb terminology. It is conceived to look for muons with a high transverse momentum, as a signature of a B meson decay. The LHCb Muon Detector consists of 5 stations along the beam axis and is based on 3-GEM (Gas Electron Multiplier) detectors for the inner part of the first station and MWPC (Multi-Wire Proportional Chamber) for the rest of the detector [2].

About 26,000 so-called "logical" channels are generated out of the 126,000 detector "physical" channels as a proper logical combination of them and sent to the L0 trigger that gives a fast response (4 μm latency) on the transverse momentum of the detector muon track. This logical combination must be done in agreement whit the space granularity used by the trigger logic that is coarser than that used at the detector level to minimize sustainable noise level and detection rate per channel.

A muon track is identified by five space point (hits), one per station, aligned and pointing to the vertex region (interaction point). In order to have a good trigger performance a 95 % detection efficiency in muon identification is required, which reflects an 99 % detection efficiency per muon station.

The LHC Bunch Crossing (BX) frequency is 40 MHz (an LHCb interaction every 25 ns). The L0 muon trigger expects from the detector front-end electronics the complete binary map of the muon detector logical channels with the associated BX identifier, which defines the event time. This information is to be supplied every 25 ns. Both the trigger and the read-out electronics work synchronously according to a pipelined architecture [3].

In order to assign the correct BX identifier, it is necessary to equalize all the different contributions to physical channel signal delays, channel by channel, before sending the information to the trigger. The main contributions to channel delays are due to the time of flight of the particles (the distance between the first muon station, called M1, and the last one, M5, is about 7 m) and the cable lengths (there are 10-15 m from the front-end channels to the read-out electronics). Also we have to consider another important point: the specific time resolution of the detectors (MWPC and 3-GEM) and the associated front-end electronics, which corresponds to a typical RMS of 3÷4 ns (Fig. 1). In order to avoid that the tails of the time distributions are assigned to a wrong BX, it is necessary to align them inside the time window of 25 ns with a resolution of about 2 ns. So we need to measure also the phase of each hit inside a BX period and reconstruct the time distribution for each channel. These contributions can give a relative delay

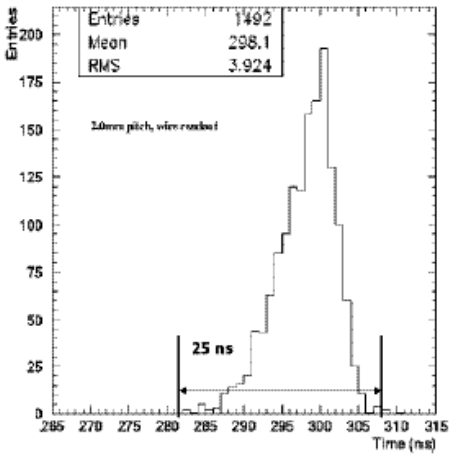

Fig. 1. Typical time distribution of LHCb MWPC channel.

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Sandro Cadeddu and Adriano Lai are with the Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari, Cittadella Universitaria - 09024 Monserrato (Cagliari) - Italy.

Caterina Deplano is also with the Physics Department, University of Cagliari, same site.

Caterina Deplano is the corresponding author (e-mail: caterina.deplano@ca.infn.it)

between different channels and more then one BX must be compensated. We divide the total delay compensation Δt in two parts:

$$\Delta t = \Delta t_C + \Delta t_F$$

where Δt_C is called the *Coarse Delay* and Δt_F is called *Fine Delay*. The *Coarse Delay* is an integer number of BX period and the *Fine Delay* is the fraction of the BX period to be added to center the time distribution inside a period of 25 ns. Using these informations it is possible to put in time every single channel of the LHCb Muon Detector and ensure the required trigger efficiency.

For practical reasons the Δt_C is compensated at the end of the Muon Detector electronics chain by an ASIC named SYNC [3], while the Δt_F is compensated on the front-end, at the beginning of the chain, by DIALOG using programmable delays.

II. DIALOG ARCHITECTURE

DIALOG (Diagnostic, time Adjustment and LOGics) is a custom integrated circuit developed in CMOS IBM 0.25 μm technology.

DIALOG will work just after the Amplifier Shaper Discriminator (ASD) chip, called CARIOCA (Cern And RIO Current Amplifier) [4], both these chips are mounted on the Muon Detector front-end board, named CARDIAC (CARioca and DIAlog Card). In each CARDIAC one DIALOG serves two CARIOCA, each one placed on a different chamber layer, for a total of 16 LVDS input physical channels.

Each single channel of the 16 DIALOG input channels can be delayed by a 31 programmable steps of $\sim$ 1.6 ns provided by a VCDL (Voltage Controlled Delay Line) as explained in section III.

It is possible to put a mask to each input channel to select (de-select) each one.

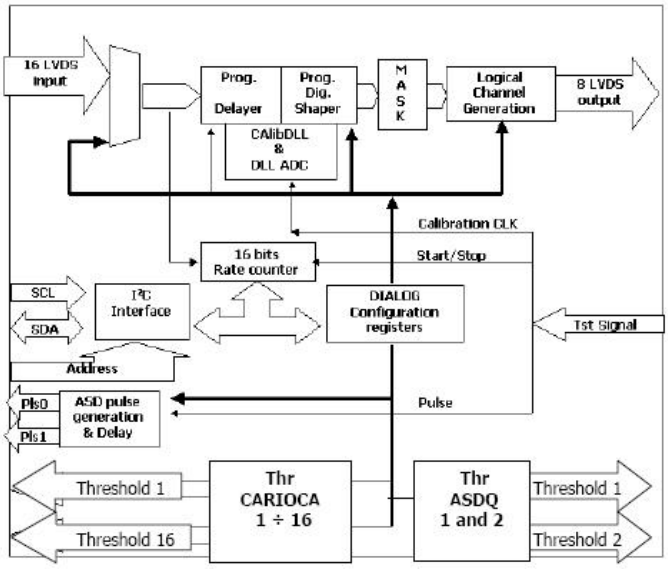

Fig. 2. DIALOG internal scheme.

DIALOG contains the logics to reduce the physical channels into logical ones. The specific logic function has to be selected between a number of configurations, according with the channels positions on the Muon Detector.

DIALOG provides 18 independent threshold signals for the ASD discriminators, using for each an integrated 8-bits DAC and a linear output driver.

DIALOG integrates also tools used for system control and diagnostic. Sixteen 24-bits rate counters are integrated to monitor the front-end rate and noise. It is possible to generate an internal pattern to test the DIALOG data acquisition chain. Finally DIALOG creates two independent pulse signals to test the ASD chips.

All DIALOG facilities are configured by the I^2C interface [5] and the control data are stored inside a 93 $\times$ 8 RAM. Each DIALOG has 7 bits address, 3 of which are fixed, so the longest I^2C chain contains 16 DIALOG.

The basic DIALOG functional units are illustrated in Fig. 2. Following the data path we can identify: 16 LVDS physical input channels, a multiplexer selecting either the input signals or a pattern stored inside DIALOG registers, delayers and digital shapers, the masking block and finally the logical channels generation unit. 8 LVDS logical channels are output. After the multiplexer the signals can be sent to the rate counters for monitoring purposes. The I^2C configuration registers and logics, the threshold blocks and the ASD pulse blocks can also be required.

III. PROGRAMMABLE DELAY AND SHAPER

Each DIALOG channel has an independent programmable delayer and digital shaper. Both these circuits are based on the same delay unit cell controlled by a DLL.

We designed a classic DLL scheme (Fig. 3) formed by a Phase Detector (PD), a Charge Pump (CP) and a Voltage Controlled Delay Line (VCDL). The VCDL is composed by 16 Delay Unit. To find the correct locking voltage, for which the unit of time delay is about 1.6 ns, we send a 40 MHz clock as "reference clock". The DLL circuit locks between a frequency (Fig. 4) of 17 MHz and 48 MHz. The main DLL characteristics are listed in Tab. I.

The 16 input channels are divided in two groups, one for each ASD chip. For each group there is a block, called ADC-DLL, which decides the time delay unit.

The ADC-DLL block scheme is showed in Fig. 5. It is designed in order to avoid the use of a free running clock but only of a calibration clock for a short period of time.

The programmable delay and digital shaper is provided, channel by channel, by a VCDL.

Before setting the programmable delay and digital shaping, it is necessary to find the correct control voltage, for which the time unit delay is about 1.6 ns (@ 40 MHz). This can be done in an automatic way, by an automatic calibration of the ADC-DLL block [3]. The main ADC characteristics are listed in Tab. II. The ADC-DLL block needs the reference clock for about 3 μs and no clock is used during normal operating conditions.

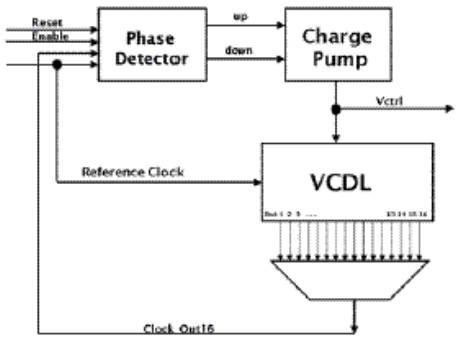

Fig. 3. DLL scheme.

The number of steps used to set the programmable delay and digital shaping is configured via the I^2C interface.
The delay of each input channel is programmable by 31 steps, while the width shape by 8 steps. Using the nominal reference period of 40 MHz the maximum delay is 50 ns while the maximum possible delay is 120 ns. The signal width can be programmed up to 28 ns and the typical width shape is 25 ns. The main characteristics of the programmable delay and digital shaping are summarized in Tab. III.

IV. ASD Threshold Signals

Eighteen 8-bits resolution DAC, based on a R-2R structure, are implemented inside DIALOG, in order to generate and control the threshold signals for the discriminators of both the ASD chips placed in the CARDIAC board. The DAC circuit is the same used for ADC-DLL block. The DAC layout is shown in Fig. 6, while the DAC characteristics are listed in Tab. IV.
When the last version of DIALOG was submitted for the production two ASD chip were candidate for the Muon detector front-end electronics: the ASDQ [6] and the CARIOCA.
We designed DIALOG to be compatible with both.
Each CARIOCA channel need an independent threshold signal. The ASDQ need only one threshold signal.

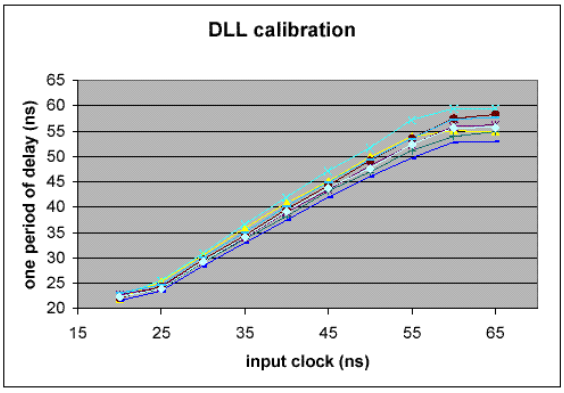

Fig. 4. DLL characterization of four DIALOG using different clock. Is plotted one period of delay versus the period of the reference clock.

TABLE I
Main DLL characteristics

Locking Time	< 500 ns
Locking Range	$17 \div 48$ MHz
Nominal Frequency	40 MHz
DNL (peak to peak)	$\pm$ 0.3 LSB

TABLE II
Main ADC characteristics

Resolution	< 8 bits
Architecture	SAR
Conversion Time	$< 2\ \mu s$
Area	$442 \times 178\ \mu m^2$

TABLE III
Main programmable delay and digital shaper characteristics

	Delay	Digital Shaper
Number of Steps	31	8
Unit Time Delay @ 40 MHz	1.6 ns	3.4 ns
Temperature Effect	50 ps/Celsius	
DNL (peak to peak)	$\pm$ 0.3 LSB	$\pm$ 0.2 LSB

The threshold voltage value used by CARIOCA and ASDQ is different. CARIOCA use a threshold voltage around 800 mV while ASDQ around 300 mV. These thresholds voltage level can be set in a range of $(625 \div 1200)$ mV for CARIOCA and in a range of $(0 \div 625)$ mV for ASDQ. The variation chip to chip of the threshold signals spread voltage is less than 24 mV (Fig. 7).
Also the input impedances of the ASD chips are different: about 24 kΩ for each CARIOCA channel and about 1 kΩ for ASDQ. So for each threshold also a buffer to drive the voltage signal is implemented. We design two linear output driver, one for CARIOCA and the other for ASDQ, to optimize the power consumption. Both contain 3 amplification stages. The main characteristics of the thresholds block are listed in Tab. V.

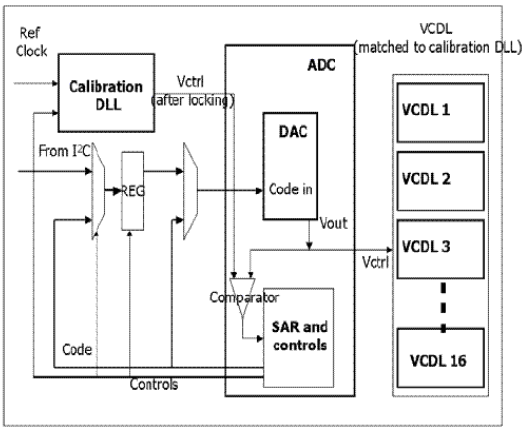

Fig. 5. ADC-DLL scheme.

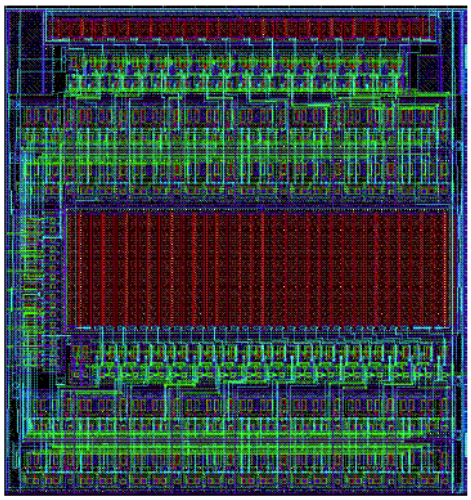

Fig. 6. DAC layout.

V. Test and Debugging facilities

DIALOG integrates a number of dedicated facilities for test and monitor purposes.

A. Pattern Generator

A 16-bit pattern can be stored in the DIALOG RAM and sent as input to test the data acquisition chain.

B. Rate Counters

Inside DIALOG there are two independent rate counters blocks, one for each ASD.
Each block has eight 24-bits rate counters:

- one, with triple voted registers, which can monitor a selected channel (one of the eight physical input channels);
- seven, without triple voted registers, that are fixed.

The rate counters can be read and reset via the I^2C bus.

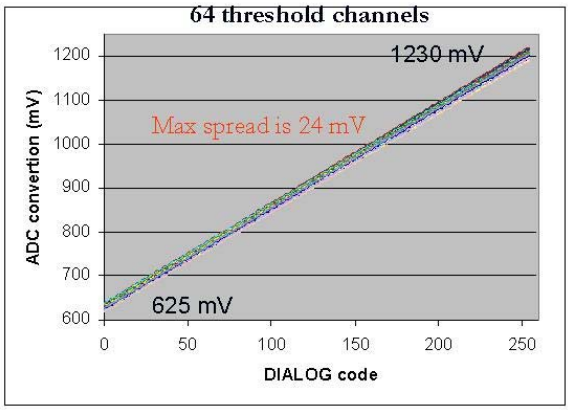

Fig. 7. Are plotted 64 threshold voltage signals value for each DIALOG DAC code. The maximum voltage spread is about 24 mV.

TABLE IV
Main DAC characteristics

Resolution	8 bits
Area	146 × 153 μm^2
DNL (peak to peak)	± 0.4 LSB
INL (peak to peak)	± 0.4 LSB
Power Consumption	± 500 μW (average)
Output Resistance	∼ 30 kΩ
Settling Time (@ 0 pF load)	50 ns max
Settling Time (@ 5 pF load)	250 ns max
Output = $\frac{(V_+ - V_-)}{256} \times code$	V_+ = Positive Supply Voltage V_- = Negative Supply Voltage
Power Supply for ADC-DLL for CARIOCA for ASDQ	 V_-=0 and V_+=2.5 V V_- =625 mV and V_+=1.2 V V_-=0 and V_+=625 mV

TABLE V
Main thresholds block characteristics

	CARIOCA	ASDQ
Threshold Signals	8×2	1×2
Impedance Load R_L	∼ 24 kΩ	∼ 1 kΩ
Good Linearity and Uniformity	$R_L > 6.8k\Omega$	$R_L > 1k\Omega$
DNL (peak to peak)	± 0.5 LSB	± 0.5 LSB
Operating Threshold	∼ 800 mV	∼ 300 mV

C. ASD Pulse Signals

DIALOG can generate two independent pulse signals. This allows pulsing the two ASD chips under DIALOG control. It is possible to select the ASD input channels to be pulsed (even, odd or both). It is also possible to delay the pulse generation. The delayers are the same that are used for the input physical channels and are controlled by the same ADC-DLL.

VI. Behavior under radiation

DIALOG is realized in IBM 0.25 μm using radiation-hardening layout techniques (enclosed gate structures) [7]. This technology is proved to resist up to tens of Mrads without significant performance loss. The highest dose to be sustained in the Muon System front-end is around 1 Mrad in 10 LHC years, on the inner part of M1 station.

Concerning Single Event Effects (SEE), DIALOG uses a triple-voted structure for all the configuration registers and the state machine registers. Each register is triplicated and the data is provided by a majority OR. Moreover, the configuration registers are also endowed with a self-correcting logic circuit.

The previous version of DIALOG, called DIALOG-β, has been tested against the SEE at the PSI (Paul Sherrer Institute). We used a 250 MeV protons flux of $6 \cdot 10^8 cm^{-2} s^{-1}$ and collected a fluence of 10^{13} protons cm^{-2}. During the test all DIALOG registers were continuously written and read back via I^2C.
No SEE has been detected.

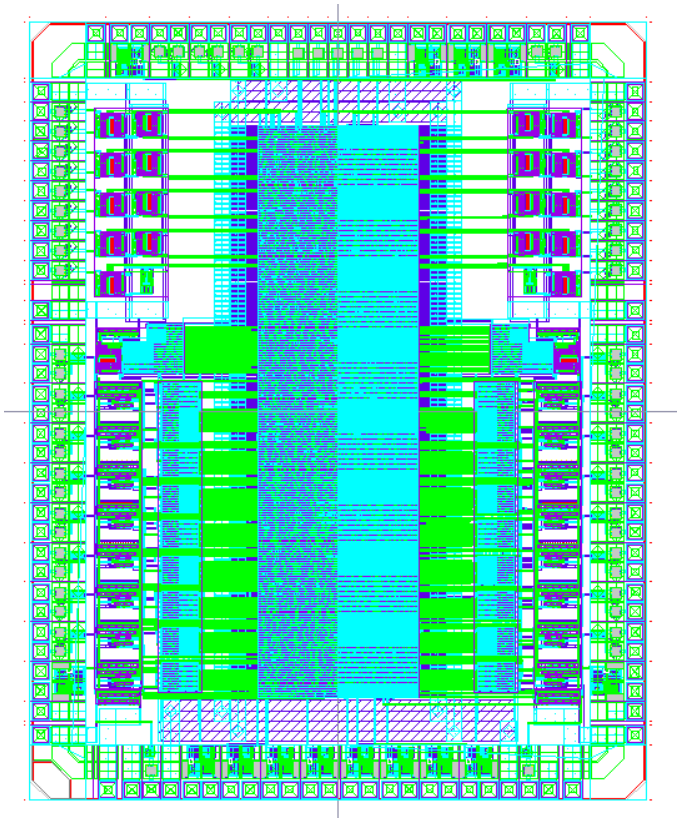

Fig. 8. DIALOG layout.

We tested also the final version of DIALOG, called DIALOG 1.0, against accumulated dose at the Hospital *R. Binaghi* at Cagliari. The chip integrated 1 Mrad using a system of six Cs 137 γ sources. After source exposure the chip worked properly.

VII. Conclusion

We design a custom integrated circuit, called DIALOG, for the front-end electronics of the LHCb Muon Detector.
DIALOG integrates fundamental tools required for the Muon Chambers time alignment and monitoring and for the Muon Trigger operations. It also provides many other features for system control and diagnostic.
In Fig. 8 is shown the DIALOG 1.0 die. Some DIALOG 1.0 characteristics are listed in Tab. VI.

We successfully test all DIALOG 1.0 features with a dedicated test bench. Also DIALOG 1.0 was completely tested under the final operating condition, on the CARDIAC board in a fully equipped MWPC, both in the laboratory and at the CERN gamma irradiation facility.
All DIALOG functionalities work properly.

TABLE VI
DIALOG characteristics

Pins	113
Power Supply	V_- = 0 and V_+ = 2.5 V
Power Consumption	50 mA (average)
Area	3875 $\times$ 4900 μm^2

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