New Architecture of Network Elements

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Abstract: This paper describes design and computer simulation of a new architecture of a node active network element, based on artificial neural network technology with the support of priority processing for different connection types. As an example of a network element was selected switching area. This network element with optimized switching area is able to transfer large data quantity with minimum delay. Architecture of network element, that contains artificial neural network for optimized priority switching is described in this paper. It describes implementation of neural network in control process for data units switching. The programming language MATLAB 7.0 was used for software simulation. Network elements with new architecture, which uses a neural network, as well as intimated simulation, are suitable for working for example in personal wireless network communication systems.

Keywords: Neural network, Switch, Switching area, Network element, Neuron

1 Introduction

The switching-over is the basic function of the active network elements that work above physical layer of OSI model. The function of switch consists at that, so data incoming on inputs must be transported to target output and it what fastest. The speed can be limited by blocking, it is caused by situation when data flow from two or more inputs directs to one output. It is necessary in this case for everyone data flow to reserve fair output allocation. Basic communication protocols for computer networks, like protocol IP or Ethernet, does not contain any mechanism for controlling of fair or priority communication channel reserving and they use queue of FIFO type. As modern multimedia applications would such mechanism often need, the possibilities how to guarantee this mechanism are searched very hardly in present. The common quality of these solutions is, that it is assumed the identification of single data or groups of data flows and priority allocation, on basis that the switching process is made.

2 Model of the switch making use of artificial neural network

The basic model of switch-over switching area consists of several partial blocks. The block diagram of the switching area is illustrated on the Fig.1. The received data units are first storage into input buffer. As data units contain target address, it is possible to determine over which output port they leave switching system. Except information about target port are detected also information about data flow whereto the data unit belongs to. Mentioned information are assembled from of all data units retained in input buffers and serve as input data for neural network.

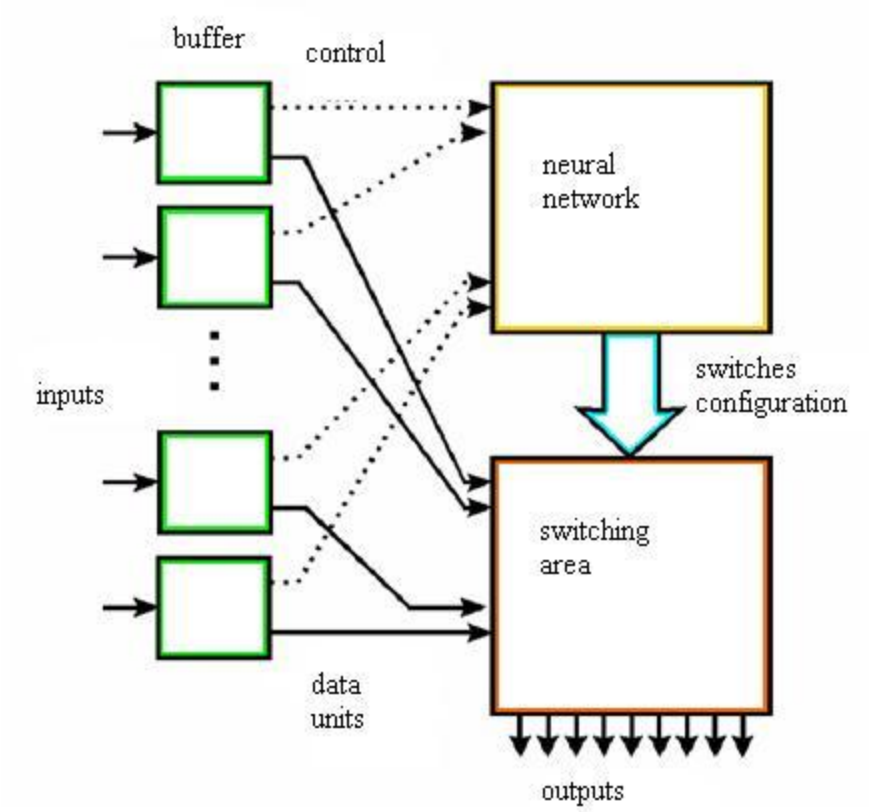

Fig. 1 Block diagram of switching area utilizing neural network

In the event of, so the frames in the port's buffer have such target addresses, so to everyone's output direction exists at most one requirement, it is possible directly put together N-dimensional vector, formed from priorities of single requirements. The first component of the vector includes the frame's priority oriented to the first output, the second one includes the frame's priority oriented to the second output and so one.

The vector must always contain concrete values. In the event of, so no requirement is to output port, have to be on relevant position of the vector the value corresponding to the lowest priority.
In the event of, so more frames in buffer are headed to the same output and it either with the same or with the different priority, have to exist way how to determine, which concrete one will be chosen for optimization process. In the event of different priority the frame with the highest priority is chosen of course. As far as the data units have the same priority, another algorithm for selection must be implemented.
It is possible from vectors of priority since single input ports to create the NxN dimensional matrix, that shall contain input conditions, to be necessary for optimize. Like answer on this input data the neural network will generate explicit configuration of switches, on basis that the switches in the switching area will be set. Generated configuration will be in the form of NxN dimensional matrix, so-called configuration matrix. Demand on generated result is to be connected always one input and one output. This condition will be projected to the configuration matrix that is generated by neural network thus, that at every row and at every column will be exactly one active output, i.e. the value is one. The other will be non-active, i.e. the value is zero. Past setting of switches it can come to own transmission of data units from input buffer units to outputs of system.
It was already states, that setting of the switches has to be optimal in light of the matrix of priority. To the configuration matrix, obtained as a result that is generated by the neural network, we can look like to a template. By the help of this template, it is possible to choose elements from arbitrary NxN dimensional matrix. **P** so, that from the matrix **P** are selected only elements, which stands on the position, where the configuration matrix has the value of one. That way we obtain from the matrix **P N** selected elements by the help of the template. When we apply this template to the matrix of priority obtained from the input buffers, we are able to determine the priority of elements, that just will be transported. We can then formulate the optimization exercise so, in order to be summation of priorities minimal. But at the same time, how it was already noted above, we have to guarantee in every row and column of matrix only one value of one. This condition is not completely accorded to the optimization travelling-salesman problem, but it is very close to it.

3 The basic scheme of the element

We think over the single-stage switching area, which has three inputs and three outputs, it is switch on the Fig.2. The switching area is realized on the cross-bar switch, i.e. in the described case the switching area with 9 switching points. We can connect arbitrary input to arbitrary output. However in one time moment t we can transfer information from one input only to one output in terms of only one's switch.

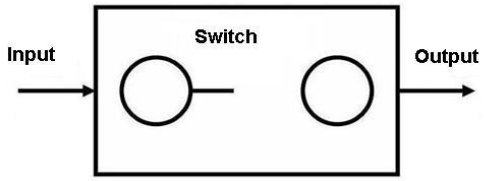

Fig.2 Switch

We create the switching area by in a way, that the switches will be shape partial positions, generally m-n dimensional matrix, in described case 3x3 dimensional one. We do not speculate about multiplexing of inputs or outputs, every switching point of the switching area presents one switch (Fig.3). The multiplexing has meaning for generally m-n dimensional switching area, main benefits have economic character, saving of a material and of a place.

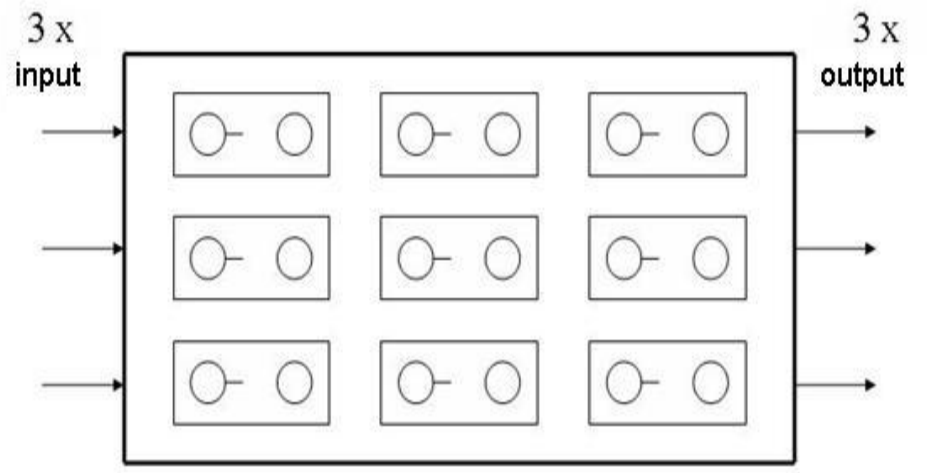

Fig.3 Switching area

The function of switching area is, in order to data unit, which reveals on the input, was transported to relevant output of the area and continues further to a receiver. As far as we would introduce data units into switching area only from one input and other inputs would be cancelled, function of all area would be greatly unused and efficiency would be small. That is why we want, to appear in the same instant of time data units on every input, which have to be transported pass through switching area. One quite serious problem is here. It can become, so on two and more inputs in the same time moment data units appear, which are addressed to the same output. Then the question

arrives, which one of data have priority of processing and for which of them is not real-time transmission critical. This question is solved by the priority processing method.

We return back to the switching area. We introduce the simplest network about so much message sources (data), how much it has inputs in the node and so much receivers, how much it has outputs. We should have only one node in the network. So that we prove to deliver the right data units to the correct receiver, we have to set up addressing. The simple two-bits addressing word, how in the event of input, that way also of output of the switching area, is used in our example (Fig.4). The first input has address 01, the second one 10 and the third one 11. The first output has address 01, the second one 10 and the third one 11. The resolution, whether or not it walks about input or output address, is given by virtue of the data frame header, where it is stated, whether it walks about source or target address. The priority is stated also in the header. The frame structure is on the Fig.5,

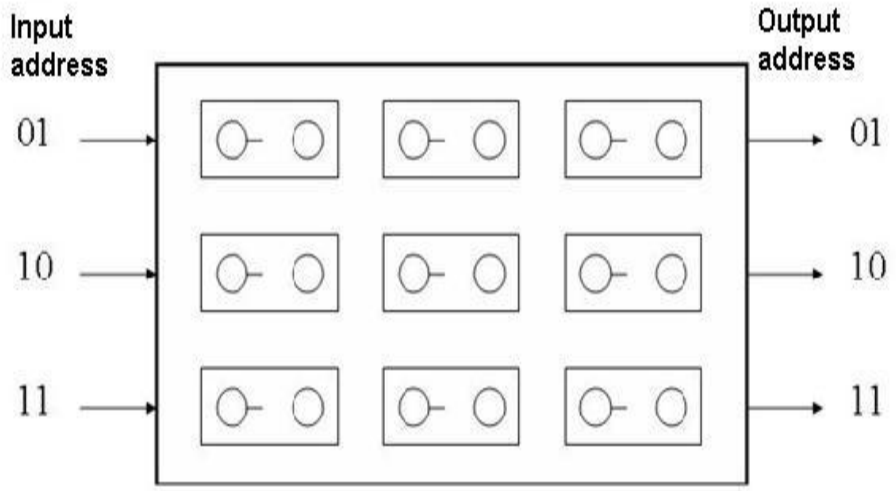

Fig.4 Switching area with addressing

2 bits Target address	2 bits Source address	4 bits Priority	16 bits Data

Fig.5 Frame structure

4 Control of switching area

The switching area would not be operational without control. The control is here realized by control matrix, which has dimension of switching area and every element of this matrix control one switching point. It is matrix with the dimension 3x3, in described case.

$$\mathbf{C} = \begin{pmatrix} x & x & x \\ x & x & x \\ x & x & x \end{pmatrix} \qquad \textbf{(1)}$$

Indexing of switching area according to control matrix **C** is simple. The switching point, which switches the first input, i.e. with the address 01, to the first output (address 01) corresponds to the matrix element with the index 11 (C_{11}). And farther, the switching point which switches the first input to the second output will be operating by the element of control matrix with the index 12 (C_{12}), etc. The elements of the matrix put on binary value 0,1. The value of logical 1 means bracing of the switching point and thereby the way through the switching area is closed and data units from the appropriate input are transported to the given output. The switching point, controlled by the appropriate element of matrix about the value of logical 0, will be in a sleep position, the switch does not close and it means, so the data units from appropriate input were routed to other output. On the Fig. 6 we can see the particular graphic example. The outputs of switching area are for simpler notion removed from the right side to low one, because on the original picture is not clear, which switching point corresponds to which output. The control matrix will be given by elements:

$$\mathbf{C} = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix} \qquad \textbf{(2)}$$

It is given, at this structure of control matrix, so logical value 1 of the matrix element C_{12} switches switching point, which connects the first input to the second output. Further the logical value 1 of the matrix element C_{21} switches switching point which connects the second with the first output and last the logical value 1 of the matrix element C_{33} switches switching point which connects the third input with the third output.

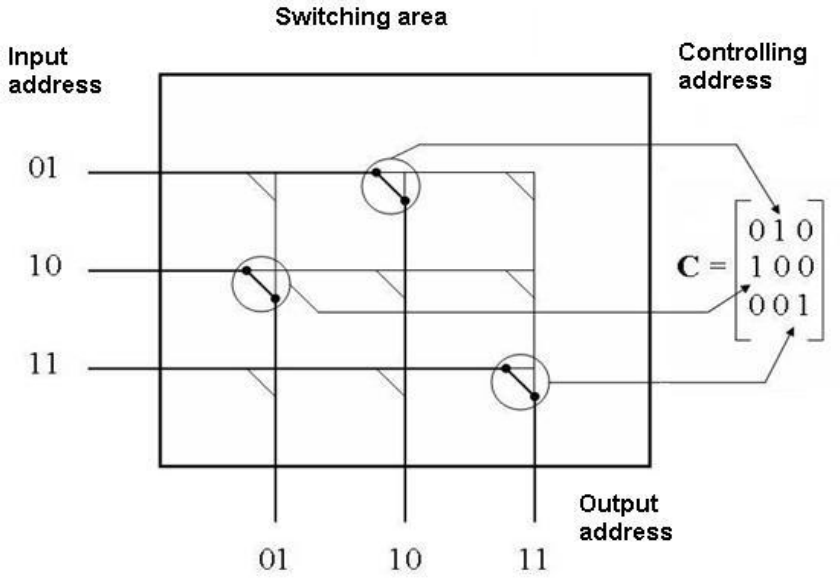

Fig.6 Switching area controlled by control matrix

5 Scheme of neurons examining priority selection

The most important part of the whole network element is a block, which examines priority selection of frames. This frames will be subsequently sent to the switching area. The block by virtue of certain information evaluates the most acceptable or rather the most important frame from the possible selection and gives up advice for sending it. Just this block works on the principle of neural network. The neurons practise this important priority selection. The scheme of neurons examining priority selection in on the Fig.7.

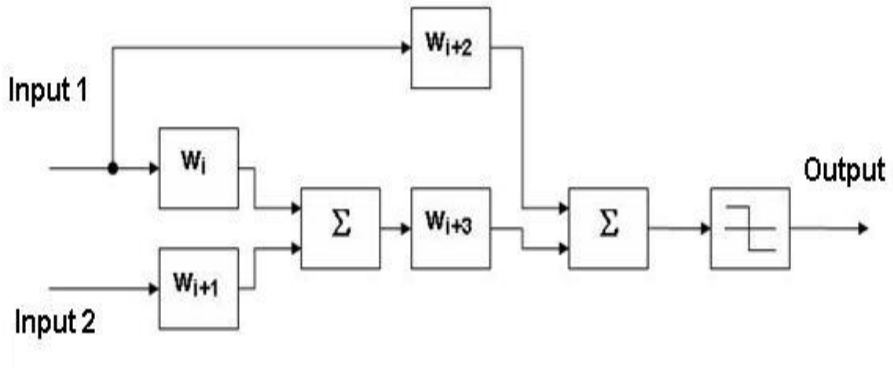

Fig.7 Scheme of neurons examining priority selection

The block, that examines priority selection, contains from two neurons. This block selects within one output of switching area if you like of one output address. For our actual switching area, and consequently 3 possible output addresses, 3 these blocks will be used. The values of priority of single frames, which ask for input to the switching area, are set to the input of the block. The frames have one sharing, all frames have the same final address as well as different source address. It comes to this, that frames from different directions are routing to the one particular output. So that we decide, which frame to choose, we have to compare their priority. At the beginning we take priority from frames, which are on the first two inputs, during which time the priority of frame, which applies approach to the first input of switching area, will allocate to the input 1. The first neuron these two priority sums and numbered value sends to the second input of the second neuron. On the first input of the second neuron we send priority from the input 1. The result is sent to the block of non-linear function after numbered of both values to the summarize block of the second neuron. It decides, whether on the output will be value log0 or log1 and all process repeats. The value of output controls partly the assignment of priority to the inputs one and two as well as the associated matrix of priority **B.**

6 Conclusion

The aim of this research was assembling of theoretical materials and knowledge concerning to the problems of network elements and artificial neural networks and then design and subsequently computer simulation of a new architecture of node active network element. This network element will be founded on the technology of artificial neural networks and will support priority processing of different types of

connection. The optimization of switching area of these active elements is very actual. In the paper is stated the architecture of network element, which includes neural network for optimizing of priority switching. It was used programme language MATLAB 7.0 for the software simulation. The idea of the implementation of neural network at control process of switching of data units is indicated at simulation. It is also during the simulation demonstrated, to what purpose is every bloc in the element used.

At last it is possible to claim, so target of the research were realized. It was designed a simulated network element, containing in the process of control of switching area artificial neural network. The element further switches single data units making provision for priority. The next research will be expansion of the number of inputs and outputs of the network element.

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