IMAGE PROCESSING BY A 0.3V 2MW COARSE-GRAINED RECONFIGURABLE ACCELERATOR CMA-SOTB WITH A SOLAR BATTERY

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ABSTRACT

Cool mega array with silicon on thin box (CMA-SOTB) is an extremely low power coarse grained reconfigurable accelerator. It was implemented by using the SOTB technology developed by a Japanese national project, low-power electronics association & project (LEAP). Making the best use of such a device and low energy architectural techniques, CMA-SOTB works more than 25MHz clock with less than 0.3V supply voltage. Various optimization can be done by controlling the body bias voltage for PE array and microcontroller independently.

The demonstration using CMA-SOTB first shows that a simple image processing application can work with 0.25V-0.4V solar battery. Then the leakage power control by changing the body bias is demonstrated. In the stand-by mode, less than 20μW power is consumed by using strong reverse bias.

1. INTRODUCTION

Extremely low power operation is widely required for cencer networks or wareable computing. Sytems have to work almost externary with a simple buttun battery or solar battery. Traditionally, a tiny CPU that works in the near threshold level operation has been used with extremely low frequency (less than 10MHz) for such a purpose. However, recently, even for such application, a certain computational performance is needed, and the performnance of such a simple CPU cannot afford it. Coarse graind reconfigurable arrays (CGRAs) have receive the attention as low power accelerators to achieve enough performance by combination with a low power CPU. One of such CGRAs, called cool mega arrays (CMAs)[1][2][3] have been developed and improved to reduce the energy as possible.

The newest version of CMA is called CMA-SOTB[3] that uses a brand new semiconductor technology called silicon on thin berried oxide (SOTB), develped by a Japanese national project, low-power electronics association & project (LEAP)[4]. It is an advanced silicon on insulator (SOI) technology, in which transistors are formed on top of a thin insulator. It can work with a much lower supply voltage than that for bulk CMOS transistors. Also, the leakage current and delay of the transistors can be controlled by using the body bias.

CMA-SOTB works more than 25MHz with exteremely low supply voltage, 0.25V, and by using strong reverse bias, stand-by power can be less than 20μW. In CMA-STOB, body bias voltages are independently supplied to PE array and microcontroller. By optimizing their balance, a high energy efficiency is achieved.

The goal of the demonstration is showing that CMA-SOTB really works with low voltage supply and the trade-off between leakage power and performance can be managed by the body bias.

2. CMA-SOTB

2.1. SOTB CMOSFET

One of useful features of silicon on insulator (SOI) CMOS technology is balancing the trade-off between the performance and leakage power with the low voltage supply. Unlike in conventional bulk CMOS, in SOI, transistors are formed on top of the insulator(typically SiO_2). By surrounding the transistor with insulating material, the electrical interference does not need to be considered, and the electric characteristics become sharp[5]. The SOTB (Figure 1) is a type of SOI, but the transistors are formed on thin BOX (Buried Oxide) layer.

By using the BOX layer, the detrimental short channel effect (SCE) can be suppressed in the SOTB. Since impurity doping (halo implant) to the channel is not necessary, the variation of the threshold voltage by the RDF can be reduced. Multi-threshold voltage design is easily available by doping an impurity into the substrate directly under the thin BOX layer. Thus, we can extensively control the range of body (back-gate) bias and optimize the performance and

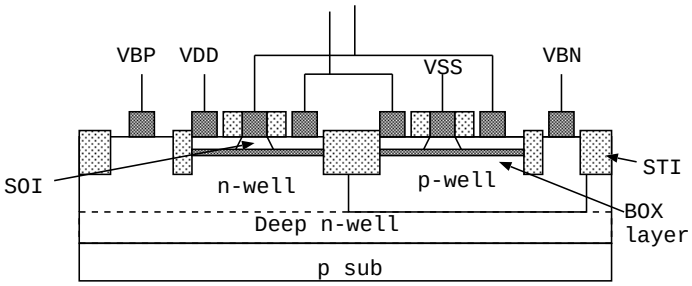

Fig. 1. Cross-sectional view of the SOTB Device

power consumption after fabrication.

The characteristics of SOTB are summarized as follows: (1) The junction capacitance of the SOI is about 1/10 that of the bulk, thus making high-speed operation possible. (2) The latch-up is not caused since a parasitic thyristor in bulk CMOS is not formed. (3) Anti-radiation tolerance is high. (4) Noise propagation (cross-talk) is small because of the insulation.

The detail of SOTB technology and prototype chips are shown in the articles[6][7].

2.2. CMA-SOTB

A key concept of CMA architecture is reducing any energy usage other than that required for computation[1]. The PE array is built with combinatorial circuits to eliminate the power needed to store the intermediate results in registers and to clock distribution to each PE. Registers are only provided at the inputs/outputs of the PE array, and computation starts when all data are set up in the input register and the outputs of PE array are stored into the output registers with a certain delay time. In order to avoid the energy for dynamic reconfiguration, we map the dataflow of the application statically on the PE array.

In order to solve various application programs only with a static data-flow, a microcontroller is provided to read the data from the data memory (DMEM) and distribute to the register attached to the input of the PE array. It also collects the results from the register attached to the output of the PE array, and writes them back it to the data memory. The computation in the PE array and the data management by the microcontroller are performed in a pipelined manner.

Figure 2 shows the architecture of CMA-SOTB. The PE array network of the CMA-SOTB is a combination of two-channel island-style interconnection and direct links that connect to the north-east and east of the PE.

Another key concept of CMA is improving the energy efficiency by balancing the computational performance in the PE array and data transfer performance between memory systems by the microcontroller. The original CMA-1 uses

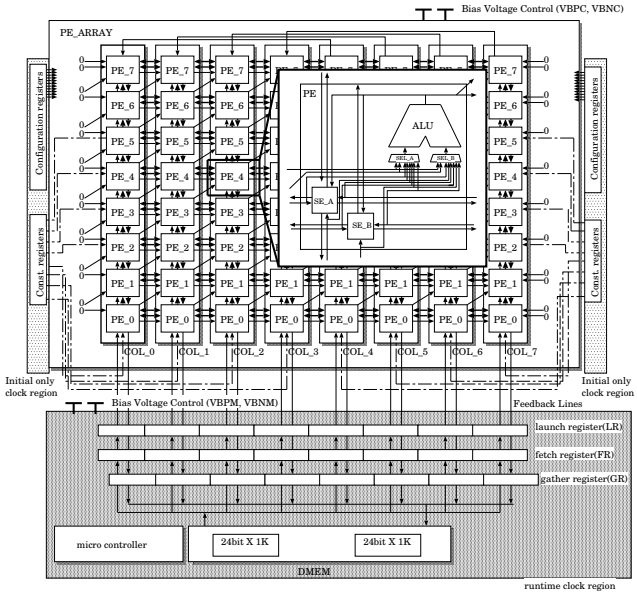

Fig. 2. Block diagram of CMA-SOTB

voltage scale control to keep this balance. If the computation is faster than the data transfer time, the voltage supplied to the PE array can be reduced. The total power required for computation can thus be reduced without degrading computing performance. On the other hand, if the data management delay is shorter than the computation delay, wave pipelining in the PE array can also be used[1]. However, this policy is not suitable when the power supply voltage is lowered as possible. The further decreasing the supply voltage will cause drastic performance degradation.

2.3. Controlling body bias voltages

As shown in Figure 1, an SOTB transistor has a back-gate bias contact provided to its well. By controlling the bias voltage, the threshold of transistors is changed. For an NMOS transistor VBN is given to its p-well. Here, zero bias (VBN=0) means the transistor works with its normal threshold. When reverse bias (VBN of negative value) is given, the threshold is increased and so the leakage current is reduced but the delay is stretched. In contrast, with the forward bias (VBN of positive value), the threshold is decreased and so the leakage current is increased but the operational speed is enhanced. For PMOS transistors, the threshold can be controlled by complementary voltage.

In CMA-SOTB, the bias voltage is implemented independently for the PE array and microcontroller. Thus, the performance and leakage power of them can be controlled independently. The policy of setting the power supply voltage and bias voltage discussed in [3] is summarized as follows:

- In the stand-by mode, strong body bias should be given for both PE array and the microcontroller. The leakage power can be suppressed less than 20μ W.

- By required clock frequency, the power supply voltage should be decided. If the target frequency is less than 30MHz, use 0.3V. From 30MHz to 80MHz, 0.4V is suitable. When the target frequency is more than 80MHz, use 0.5V or more.

- Choose the body bias for PE array small as possible in the range to satisfy the required performance. Then, decide the body bias for microcontroller small as possible in the same manner.

3. DEMONSTRATION OVERVIEW

In order to demonstrate the low power operation of CMA-SOTB, we prepared a system with a solar battery. Figure 3 shows demonstration environment overview. The solar battery generates the power of 0.5V at maximum. A simple image processing application program is working on CMA-SOTB with supply voltage of the solar battery, and result image is continuously shown in the display. The operational frequency is 25MHz.

The supply voltage is controlled by changing the distance between the electric light bulb. Thus, we can change the voltage by moving the light bulb, and show how much supply voltage CMA-SOTB stops working by checking the voltage meter. CMA-SOTB will stop working around 0.25V, but since the state is saved, it can start again when we move the light bulb closer. By showing an ammeter at the same time, its small consuming power can be also demonstrated.

The next demonstration is to show how the leakage power can be controlled by the bias voltage. We provide two sets of bias voltage and they can be selected by the switch. Just by switching it, we can show the leakage power becomes extremely low in the stand-by mode but the state is still saved.

Figure 4 shows a photo of the demonstration board. The CMA-SOTB is the first practical fabrication of the SOTB process, and the testing board is only designed for power and performance measumement of the target chip. Since there is no available I/O for demonstration, we must connect the testing board to another board providing the VGA driver and connecter with hand-made wires. As a result, we need two small SPARTAN-6 FPGA daughter boards for the interface. One board manages the input/output of images from/to the CMA-SOTB chip, and the other daughter board is used just for the interface of VGA output. The power for these two FPGA boards is supplied from another power supply, since they need much more power than that for CMA-SOTB and the solar battery cannot afford it.

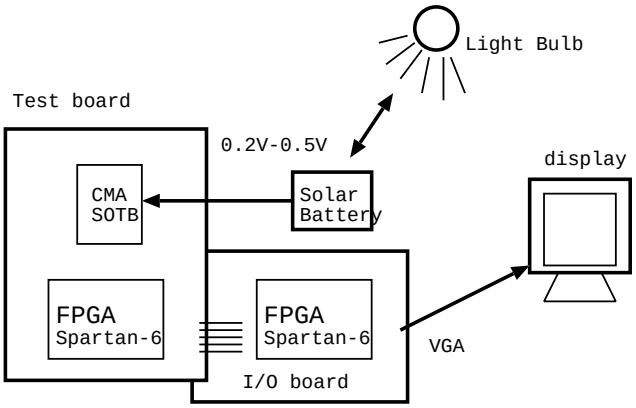

Fig. 3. Demonstration environment overview

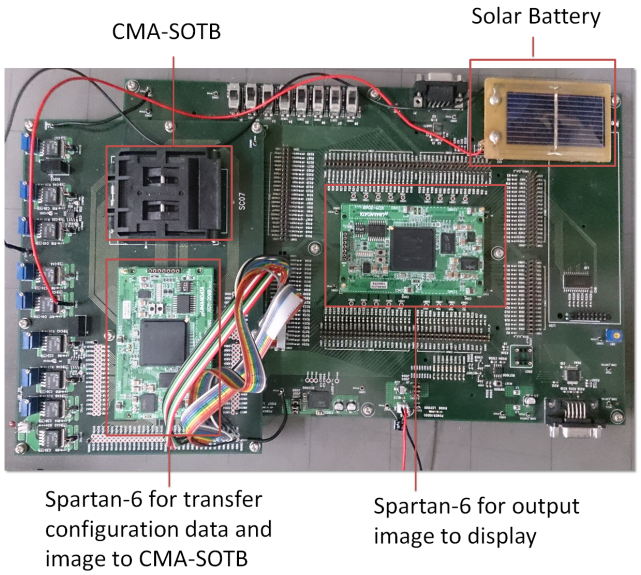

Fig. 4. Photo of the Demonstration system

4. SUMMARY

Image processing demonstration by the CMA-SOTB with solar battery will demonstrate that it works normal clock frequency with extremely low power supply. The effect of changing body bias will be also shown, and its extremely low leakage power in the stand-by mode will be demonstrated.

Now, we use two mother boards each of which has its own SPARTAN-6 FPGA daughter boards connected with hand-made wires. They make the demonstration system large and power consuming. Now, the new testing board with I/O is under development. If it is in time, we can use a simple board with a SPARTAN-6 FPGA daughter board managing everything.

Acknowledgment

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