3D bus architecture using inductive coupling ThruChip-Interface

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1 Introduction

In recent years, 3D chip stacking attracts attention in terms of reducing the chip area while maintaining performances. To make use of the flexibility of 3D multiprocessor, it is significant to communicate between the stacked chips wirelessly. ThruChip-Interface (TCI)[1] is the inter-chip communication interface using inductive coupling between the inductors on the stacked chips. By applying TCI to the communication in the 3D multiprocessor and communicating wirelessly for interconnection between the stacked chips, the replacement/addition/deleting of the chips are enabled and then high flexibility is provided.

Here, we propose an asynchronous bus and a resonant synchronous bus as feasible methods to decrease the latency of communication with the 3D shared bus.

2 3D bus for TCI

To operate 3D multiprocessor with low latency, the way to interconnect between the chips is significant. 3D shared bus is suitable method because it needs only one hop for communicating between any two chips. Moreover, as Fig.1 shows, 3D shared bus enables broadcast communication in the whole stacked chips.

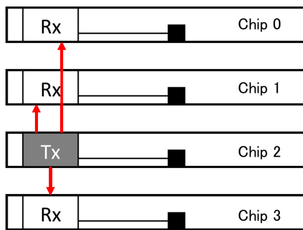

Figure 1: 3D shared bus (Tx: transmitter Rx: receiver)

However, in 3D shared bus applied TCI, a method using arbitration like Dynamic TDMA is not available because it needs an arbiter and extra TCI links to request and grant the signals. Considering a large footprint of coils for TCI, using a number of them for such signals is waste of the semiconductor area. One of the conventional feasible methods is Static TDMA bus but it tends to cause network latency owing to the waiting time for using the bus.

3 Proposed bus architecture

3.1 Asynchronous bus

The proposed asynchronous bus (async-bus) is shown as Fig.2. Communication in the async-bus is performed by CSMA/CD. In the TCI bus, each chip can check the bus. Unless the communication occurs at the bus, any chips can use the bus.

In this way, when one chip uses the bus to send packets at a certain time, another chip may use the same bus at the same time. Then the packets conflict, and the resend of the packets is necessary. In the async-bus, if the conflict occurs, each chip resends the packets after waiting for random backoff time.

3.2 Resonant synchronous bus

In resonant synchronous bus (sync-bus), the packets are synchronized with a clock. For distributing a high speed clock for multiple chips, a resonant synchronized technique[2] can be used. Therefore, a link for distribution of the synchronous clock is added.

In the communication of resonant sync-bus, each chip sends bus-request signal before it sends the packets. If the signals don't

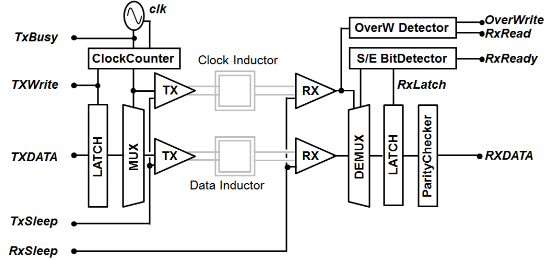

Figure 2: Intellectual property of bus architectures

conflict, the chip can send the packets at the next cycle. Otherwise, they send the packets with resend mode (Fig.3). From this method, the conflict of the packets can be avoided.

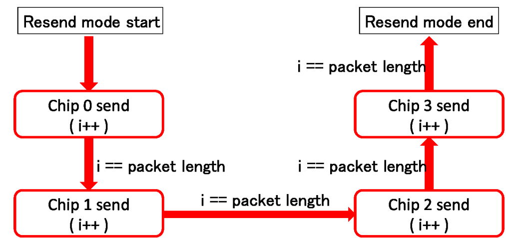

Figure 3: Resend mode (4 chips stacked)

4 Evaluation

The result of network simulation by Gem5 simulator is shown in Fig.4. Zero-load latency of the two proposed methods both reduced up to 50% from that of Static TDMA. In comparison between throuput of two proposal methods, resonant sync-bus is superior to async-bus since resend mode prevents the packets from conflicting.

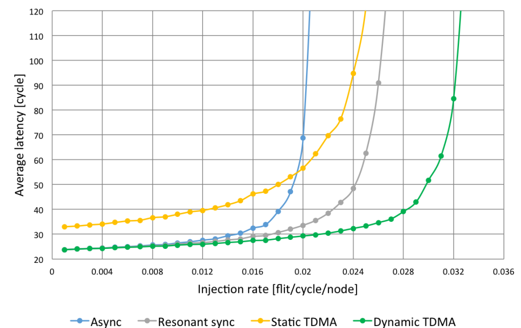

Figure 4: Network simulation (4 chips stacked)

5 Conclusion

In this report, two kinds of shared bus architecture for TCI connected 3D chip stack is proposed. Network simulation results shows that both async-bus and resonant sync-bus improved the zero-load latency of Static TDMA by 50%. Additionally, network throuput of resonant sync-bus is 1.3 times of that of async-bus with only a synchronization link.

References

[1] T.Kuroda. "Thruchip Interface (TCI) for 3D Network on Chip.", *VLSI and System-on-Chip(VLSI-SoC), 2011 IEEE/IFIP 19th International Conference, pp. 238—241, Oct 2011.*

[2] Y.Take, et.al. "3D Clock Distribution Using Vertically/Horizontally -Coupled Resonators.", *In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International, pp. 258—259, Feb 2013.*