A Leakage Current Monitor Circuit Using Silicon on Thin BOX MOSFET for Dynamic Back Gate Bias Control

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Abstract

A leakage current monitor circuit was developed for dynamic back gate bias control of CMOS LSI with Silicon on Thin BOX (SOTB) technology. By using the SOTB technology, sensors or wearable devices can suppress the leakage power by giving deep reverse body bias when they are not used. Once an event occurs, they must turn to the operational mode by changing the body bias quickly. According to the real chip evaluation, it takes hundreds of micro seconds, and the wake-up time is difficult to be estimated. The proposed detector using a leakage current monitor circuit guarantees that the target module is ready to be operational. The target body bias voltage for operation can be controlled by the bias voltage of the detector domain, which is computed with an expression in advance. SPICE simulation reveals that formulation is done and power overhead is only 42.7-42.9nW in the room temperature. Compensation equations for various temperatures are also shown. (Keywords: Leakage Monitor, SOTB MOSFET, Dynamic Back Gate Bias Scaling)

I. Introduction

Dynamic control of back gate bias has been a key technique for operating low power LSIs. Controlling the threshold level of MOSFET by using back gate bias has become much more effective in recent SOI technologies. Especially, with silicon on thin buried oxide (SOTB) [1] developed by LEAP (Low-power Energy Association & Projects), the leakage power and performance of logic gates can be widely controlled by changing the body bias. In order to make the best use of this controllability, dynamic body bias scaling (DBS) is useful for battery driven low energy devices such as sensor nodes. During the sensor is in the standby mode, a deep reverse bias is given to suppress the leakage current. Once the event happens, the body bias is switched to weak reverse bias, zero-bias or forward bias for high speed operation. The problem of the DBS is the transient time from the standby mode to operating mode. Fig.1 shows the time required for changing the body bias of the nMOS transistors from 0V to 0.4V evaluated by using real SOTB chips. According to the real chip evaluation, the transient time is widely distributed from 100μs-250μs[2]. In order to guarantee the end of transition in variability of transient time, a large time margin is required. This causes the response of the sensor to be slow. To avoid a large time margin, the end of back gate biasing need to be detected. we propose a light weight detector circuit based on the leakage current monitor, which can detect the end of back gate biasing from standby mode to operation mode. Although the similar method has been proposed and utilized for bulk technology [3][4], this cannot be utilized for SOTB LSI, since they require high voltage supply[3] or leakage mechanism is different from bulk technology[4].

II. A leakage current monitor

The simplest idea to detect that the body bias reaches a certain level is using a comparator circuit which compares the back gate bias directly with some reference voltage. However, for giving deep reverse bias, the bias becomes often high voltage or minus voltage which introduces electrostatic discharge for thin gate oxide layer. In order to avoid it, we used a leakage current monitor.

Fig.2 shows a structure of proposed leakage current monitor. Here, we show the circuit for body bias to pMOS transistor first, since the real chip evaluation revealed that the response time of the body bias to pMOS transistor (VBP) is always longer than that for nMOS transistor (VBN) [2]. The proposed leakage current monitor consists of a detection part and a differential amplifier. M1 in the detection part is put into a target macro of DBS, while the rest of part is placed on the different domain controlled by the bias voltage V_{sbn}. As VBP becomes low voltage, the current going through M1 is increased, and so the level of $VGND$ is increased. It is compared with the reference voltage $VREF$ by the differential amplifier, and if the $VGND$ is larger than $VREF, VOUT$ becomes “1” showing that the target macro is now ready for the operation. VEN is an enable signal of the detector. Here, assume that the comparator turns the output $VOUT$ to “1 when for the bias voltage of the target macro becomes VBP_{target}.

In order to cope with various requirements of performance and leakage power for the target macro,VBP_{target} must be changeable by the voltage of a control signal. In common comparators, the $VREF$ is used for such purpose. However, in this circuit, the controllability of VBP_{target} by the $VREF$ is too sensitive. That is, a small change of $VREF$ gives a large influence to VBP_{target}, and thus, stable control is difficult. Instead, we propose to use the bias voltage of the comparator domain V_{sbn} for the control signal.

Fig3 shows a waveform of VBP detector with the SPICE simulation using parameters shown in Table.1. The threshold level was evaluated by SPICE simulation of original designed transistors. Note that 1.5V of VBP is a deep revise bias, while 0.5V is a weak reverse bias for operational mode. Here, we used 0.17V of $VREF$ and 0.4V of VDD. This figure shows that the detector works enough high speed compared to the change of VBP. That is why, the output of the proposed circuit is nothing to do with variability of transient time of back gate bias and the circuit can detect the end of arbitrary transient time of back gate. A detector for the bias voltage for nMOS transistors can be built as the same manner. For the circuit, the VBN_{target} is controlled by V_{sbp}.

III. How to decide V_{sbn}

The target bias voltage of the proposed detector is controlled by V_{sb} from outside the chip. Here, we focus on V_{sbn} given for the VBP detector for the target bias voltage VBP_{target}. Although a deep reverse bias for standby mode is independent from the target macro, the VBP_{target} is depending on the circuits, area and application requirements. Our goal is selecting an appropriate V_{sbn} to set the VBP_{target}. According to [5], sub-threshold leakage current is expressed as:

$$I_{sub} = I_{off} 10^{\{V_{gs}+\eta(V_{ds}-VDD)-k_\gamma V_{sb}\}/S}\{1 - exp(-V_{ds}/v_T)\} \quad (1)$$

where, v_T is thermal voltage, η is DIBL coefficient, and k_γ is a coefficient got by linearization of threshold voltage about V_{sb}. The coefficient I_{off} is sub-threshold level current when $V_{gs} = 0$ and $V_{ds} = VDD$. Sub-threshold leakage current of M1and M2 is the same, and $V_{gs} = 0$ as the source and drain of M1 and M2 are connected:

$$I_{offn}10^{\{\eta_n(VGND-VDD)-k_{\gamma n}V_{sbn}\}/S_n}\{1-exp(-VGND/v_T)\}=I_{offp}10^{\{-\eta_p(VGND)-k_{\gamma p}V_{bsp}\}/S_p}\{1-exp((-VDD+VGND)/v_T)\} \quad (2)$$

Here, letter "n" or "p" is added to the subscript to distinguish nMOS FET(M2) and pMOS FET(M1). Here we set $VREF$ to $VDD/2$. That is, the output $VOUT$ turns to "1" when $VGND$ is higher than $VDD/2$. Thus, in equation (2), $VGND$ can be replaced by $VDD/2$ is re-written as

$$I_{offn}10^{\{\eta_n(-VDD/2)-k_{\gamma n}V_{sbn}\}/S_n} = I_{offp}10^{\{-\eta_p(VDD/2)-k_{\gamma p}V_{bsp}\}/S_p} \quad (3)$$

In the VBP detector, M1 is embedded in the target macro. So, V_{bsp} is VBP_{target} when the output $VOUT$ to "1". We can solve the equation for V_{sbn}:

$$V_{sbn} = S_n/k_{\gamma n}[log_{10}(I_{offn}/I_{offp}) - (\eta_n VDD)/2S_n + \{\eta_p VDD/2 + k_{\gamma p}(VBP_{target} - VDD)/S_p\}] \quad (4)$$

DIBL coefficient η and k_γ can be calculated as follows. Since the threshold voltage(V_{th}) of MOSFET is expressed as $Vth = Vt0 + \eta V_{ds} + k_\gamma V_{sb}$, η can be calculated from the slope of V_{th} vs V_{ds} with 0V of V_{sb}, and k_γ can be calculated from the slope of V_{th} vs V_{sb} with a fixed V_{ds}. Fig. 4 and Fig .5 show graphs of V_{th} vs V_{sb} and V_{th} vs V_{ds}, respectively. Here V_{th} of pMOS FET is shown with the absolute value. From Fig.4, it appears that η_n is 0.0332 and η_p is 0.0386. From Fig.5, $k_{\gamma n}$ is 0.17 and $k_{\gamma p}$ is 0.1223. I_{offn}/I_{offp} is determined by the channel width of MOSFET and Sub threshold slope S_n is 84mV and S_p is 73mV in this condition. Fig. 6 shows VBP_{target} vs $V_{bsn}(-V_{sbn})$ in $VDD = 0.4$V and $VGND = VDD/2$. The solid line in Fig.6 shows Equation (4) and the dash line represents result from SPICE simulation. Fig. 6 also shows we can get V_{bsn} from Equation (4) for wide range of VBP_{target} . For the weak reverse bias, for example, if VBP_{target} is equal to 0.7V, according to Equation (4) V_{bsn} should be set to -0.1563V. The difference between SPICE simulation result is only 9.6mV. The accuracy of Equation (4) is at most 13.78mV in VBP_{target}=1.2V and at the least 1.797mV in VBP_{target}=0.2V in Fig.4.

IV. Thermal characteristics and compensation

Since leakage current is sensitive to the temperature (T), thermal characteristics of leakage current monitor is needed to be analyzed. We must compensate Equation (4) considering the temperature. Assume that VBP detector works with 0.4V of VDD (that is, 0.2V $VREF$) for 0.5V VBP_{target}. Fig.7 shows the adequate V_{bsn} for each temperature obtained from the SPICE simulation. In 120∘C, V_{bsn} is 0.0434V lower than that in the room temperature. This makes VBP detector miss-detect the end of transition of VBP. However, from Fig.7, polynomial approximation of $V_{bsn}(T) - V_{bsn}(T_{room})$ can be obtained: $C(T) = -2 \times 10^{-12}T^4 + 2 \times 10^{-9}T^3 + 8 \times 10^{-7}T^2 - 0.0006T + 0.016$. Using it, Equation (4) can be compensated to

$$V_{bsn} = -S_n/k_{\gamma n}[log_{10}(I_{offn}/I_{offp}) - (\eta_n VDD)/2S_n + \{\eta_p VDD/2 + k_{\gamma p}(VBP_{target} - VDD)/S_p\}] + C(T) \quad (5)$$

In 120∘C, V_{sbn} error of this compensation is only 2.62mV from the result of SPICE simulation, and the error ratio is only 6.04%. The compensation for the process variation is our future work.

V. Power overhead

Since the proposed detector is for low power operation, the proposed circuit itself must not consume much power. Fig.8 shows dynamic power consumption (P_{AT}) in conditions of Table.1. This shows only 42.7-42.9nW power consumption is required. Since proposed detector consists of simple circuits and operates with low VDD, power consumption is low. Moreover, standby power (P_{ST}) consumption is only 0.3665nW .

VI. Conclusion

To control back gate bias dynamically, a leakage current monitor which can detect the end of transition of back gate bias. Proposed leakage current monitor can detect arbitrary back gate bias voltage by adjusting resistance ratio between M1 and M2 according to the equation. The accuracy of evaluating is at most only 13.78mV in room temperature and power over head can be ignored. The proposed detector can be used widely for the DBS of sensor networks and wearable devices.

Acknowledgment

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TABLE I: Condition of simulation

Process	LEAP 65-nm FD-SOI
Library for simulation	LEAP_SVT
V_{th} of M1-M7 from SPICE simulation	n:0.272V p:0.278 (VDD:0.4V zero bias)
Supply voltage(VDD)	0.4V
VBP voltage	0.5V(VBP_{target}), 1.5V(Standby state)

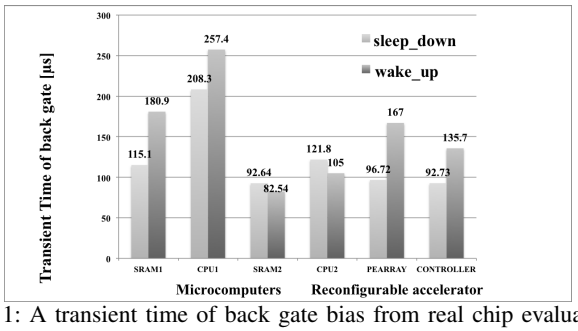

Fig. 1: A transient time of back gate bias from real chip evaluation

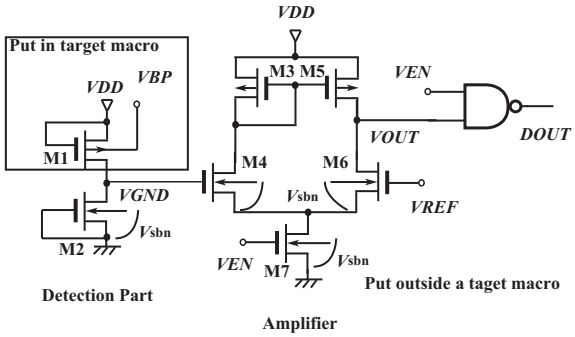

Fig. 2: Structure of a proposed leakage current monitor (this can detect a end of VBP change)

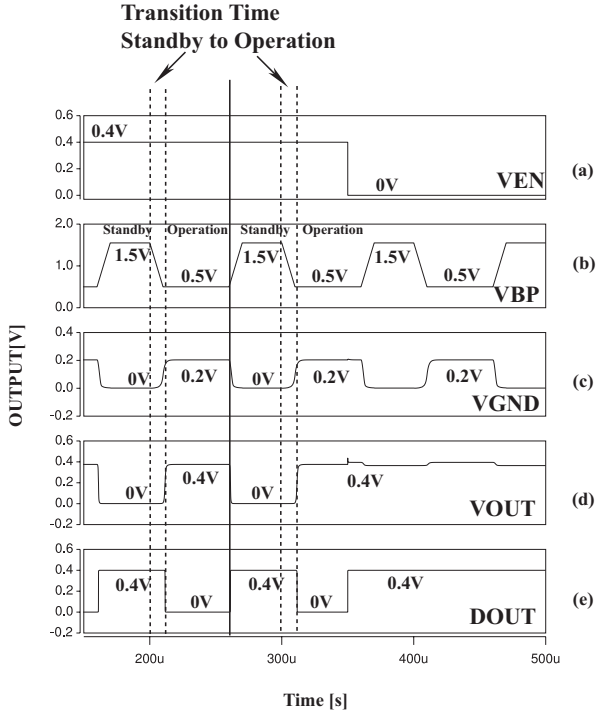

Fig. 3: Waveform of leakage current monitor(VBP detector)

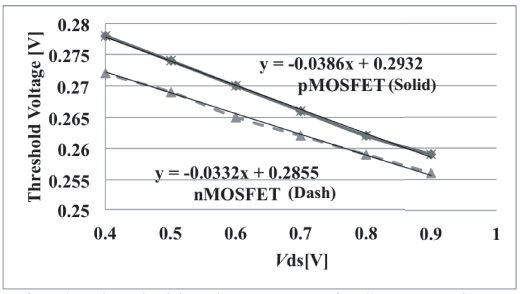

Fig. 4: Threshold voltage vs Drain-Source voltage

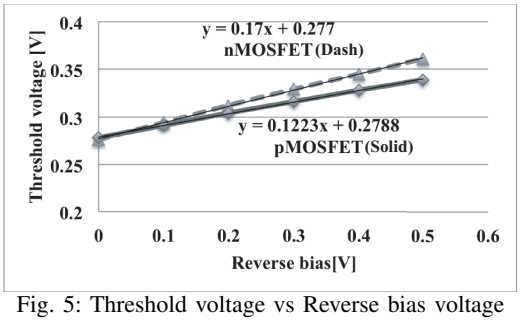

Fig. 5: Threshold voltage vs Reverse bias voltage

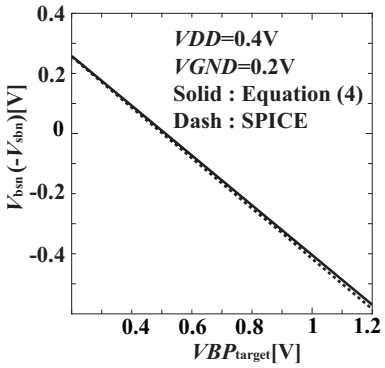

Fig. 6: V_{sbn} vs VBP_{target}

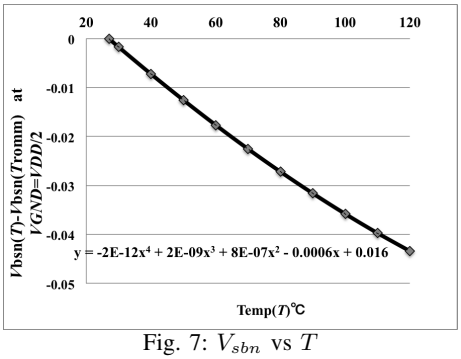

Fig. 7: V_{sbn} vs T

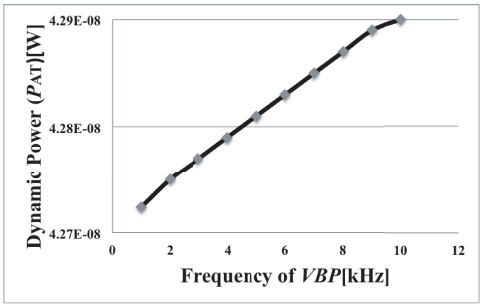

Fig. 8: P_{AT} vs Frequency of VBP