An Optimal Power Supply And Body Bias Voltage for an Ultra Low Power Micro-Controller with Silicon on Thin BOX MOSFET

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Abstract— Body bias control is an efficient means of balancing the trade-off between leakage power and performance especially for chips with silicon on thin buried oxide (SOTB), a type of FD-SOI technology. In this work, a method for finding the optimal combination of the supply voltage and body bias voltage to the core and memory is proposed and applied to a real micro-controller chip using SOTB CMOS technology. By obtaining several coefficients of equations for leakage power, switching power and operational frequency from the real chip measurements, the optimized voltage setting can be obtained for the target operational frequency. The power consumption lost by the error of optimization is 12.6% at maximum, and it can save at most 73.1% of power from the cases where only the body bias voltage is optimized. This method can be applied to the latest FD-SOI technologies.

Keywords— Body bias control, Low power design, Micro-controller, FD-SOI, SOTB.

I. Introduction

Ultra low power micro-controllers that can maintain for at least 10 years with a simple Li or solar battery are required for the latest wearable computing and sensor nodes. This performance requirement means that 32-bit microprocessors that can work with a 20 MHz or higher clock are needed instead of the conventional tiny processors near the threshold level working with a hundreds of kilo Hertz operational clock. To fulfill these requirements, a novel FD-SOI technique called silicon on thin buried oxide (SOTB) has been developed [1] and implemented on low power microprocessors [2], accelerators [3], and FPGAs [4].

An important feature of SOTB is that it can control the trade-off between performance and leakage current by changing the back-gate bias. By giving reverse bias, the leakage current can be reduced while the delay is stretched and forward bias can enhance the performance while increasing the leakage current. Thus, optimization by changing both the supply voltage and the back-gate bias is key for taking full advantage of the SOTB technique. Finding the energy minimum point by controlling both the supply voltage and the back-gate bias has been widely researched [5] [6][7]. However, from the viewpoint of designing practical systems, minimizing the energy using the lower clock, which cannot satisfy the required performance, is useless. Kao et al. [8] investigated optimization techniques from the practical viewpoint, but their study targeted only the functional units and used a conventional bulk technique. Although a CPU with the SOTB was investigated in [2], it was not based on a performance and power model.

In the present work, we propose and examine a method to find the optimal combination of supply voltage and back-gate bias for a micro-controller with the SOTB technique. The main contributions of this paper are:

- A method is proposed to optimize the supply voltage and back-gate bias for a real 32-bit micro-controller implemented with a 65-nm SOTB CMOS technique in which the core and memory are controlled independently.
- A theoretical model is proposed and examined through the evaluation results of a real chip. The accuracy of the optimization ranged from 5.23% to 12.6%.
- By applying the proposed method, the total power can be reduced by 73% without degrading performance.

The rest of this paper is organized as follows. Section 2 describes the SOTB technique with a power and performance model. The model of consumed power and operational frequency is shown in Section 3. The target micro-controller is introduced in Section 4 and the parameters of the power and performance model are obtained from the real chip measurement. In Section 5, we show optimization examples and examine the effectiveness of the proposed technique. We conclude in Section 6 with a summary and a brief mention of future work.

II. SOTB and back gate bias control

A. SOTB CMOSFET

Silicon on thin buried oxide (SOTB) is a novel FD-SOI device developed by Low Power Electronics Association & Product (LEAP). Figure 1 shows a cross-sectional view of SOTB CMOSFET. Unlike other SOI devices, CMOSFET is formed on a 10-nm ultra thin box layer. Since the FD-SOI can suppress short channel effect (SCE), impurity doping is not necessary. The variation of threshold level by the random dopant fluctuation is reduced, which is why SOTB MOSFET is suitable for operation with low voltage supply.

Since a transistor and back gate are separated by the box layer, p-n junction leakage current between drain/source and substrate is also removed. Accordingly, compared with conventional bulk CMOS processes, controllability of the back gate is improved. The triple-well structure prevents leakage current of the back gate bias control. This SOTB structure enables to change characteristics by the controlling the power supply voltage and back gate biasing.

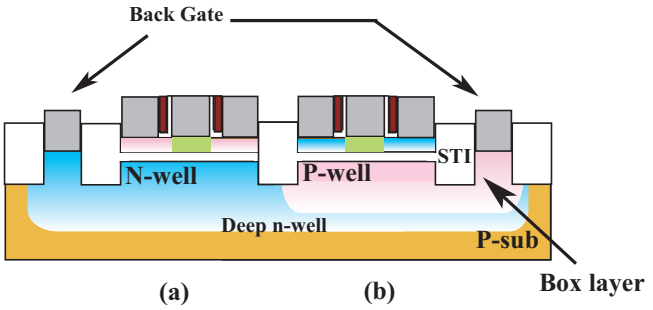

Fig. 1. Cross-sectional view of SOTB MOSFET: (a)pMOS (b)nMOS

B. Power of LSIs

In general, The consumption power of LSIs is represented as

$$P_{all} = I_{leak}V_{DD} + \alpha_{at}fCV_{DD}^2, \quad (1)$$

where I_{leak} is leakage current, α_{at} is activity factor, C is capacitance, and f is an operating frequency. The first term represents static power by the leakage current and the second one is the switching power of transistors. In the bulk MOSFET, leakage current consists of (1) sub-threshold leakage current, (2) gate tunneling current, (3) gate induced drain leakage (GIDL), and (4) p-n junction leakage current. However, in the FD-SOI structure, GIDL and p-n junction leakage current are suppressed in the normal usage[1]. So we only need to consider the sub-threshold leakage current and gate tunneling current. The sub-threshold leakage current I_{sub} is represented as

$$I_{sub} = I_{off}10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})+K_\gamma V_{sb}}{S}}(1 - e^{\frac{-V_{ds}}{v_T}}), \quad (2)$$

where v_T is thermal voltage, S is sub-threshold slope, I_{off} is the sub-threshold leakage current at $V_{gs} = 0$ and $V_{ds} = V_{DD}$, K_γ is a coefficient of the back gate bias, and η is a coefficient of the drain to source voltage[9].

The gate tunneling current I_{gt} is

$$I_{gt} = WP_A(\frac{V_{DD}}{t_{ox}})^2 e^{-P_B\frac{t_{ox}}{V_{DD}}}, \quad (3)$$

where t_{ox} is thickness of gate oxide and W is gate width. P_A and P_B are constants determined by transistor process[9]. Leakage current of the transistor is, thus, an exponential function of V_{DD} and back gate bias voltage. Figure 2 shows the leakage from the sub-threshold leakage current and the gate tunneling current in nMOSFET, including (a) the relationship to V_{DD} and (b) the relationship to the back gate biasing. Here, $VBN(VBP)$ shows the back gate bias voltage given to nMOSFET(pMOSFET). Both figures show results of SPICE simulation of ST micro's 28nm FD-SOI and 65nm SOTB. The different process technologies resulted in different the dominant leakage currents, but even so, the leakage current increases exponentially to V_{DD} and VBN independent of the process technology. In nMOSFET, when the back gate voltage (VBN) is lower than the source voltage, it is called the reverse bias that reduces the leakage current. In pMOSFET, when the back gate voltage (VBP) is higher than the source voltage, it is also called

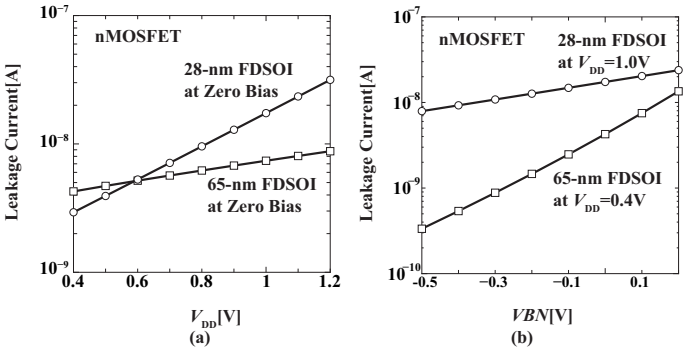

Fig. 2. Leakage current of SOTBMOSFET (a)characteristics of V_{DD} (b)characteristics of VBN

the reverse bias. Note that, with the reverse bias, delay time increases.

The leakage current also increases exponentially to V_{DD}. Note that, in the case of V_{DD}, lower V_{DD} results in lower switching power quadratic.

C. Maximum operational frequency

In MOSFET, the gate delay is represented with the α power low[9].

$$t_d = k\frac{CV_{DD}}{(V_{DD} - V_{TH})^\alpha} \quad (4)$$

Here, k is the process parameter, α is a parameter to consider velocity saturation in MOSFET, and V_{TH} is the threshold voltage. The maximum operational frequency f_{max} is proportional to the reciprocal of t_d.

$$f_{max} = F\frac{(V_{DD} - V_{TH})^\alpha}{V_{DD}}, \quad (5)$$

where F is a constant number related to frequency. The threshold voltage (V_{TH}) varies due to the back gate biasing, and it can be linearly approximated as follows:

$$V_{TH} = V_{t0} - K_\gamma VBN, \quad (6)$$

where V_{t0} is the threshold voltage with the zero bias[9]. This equation, which is for nMOSFET, but can also be used to represent pMOSFET, shows that the maximum operational frequency is also a function of V_{DD} and back gate voltage (VBN and VBP). In nMOSFET, when VBN is higher than the source voltage, it is called the forward bias that increases the maximum operational frequency. In pMOSFET, when VBP is lower than the source voltage, it is also called forward bias. Note that, the leakage current increases exponentially with increasing forward bias.

From the practical viewpoint, a system like a microcontroller must work at the operational frequency that satisfies the performance requirement. However, in most of embedded systems, extra performance is just a waste of the energy and is not needed.

Therefore, V_{DD} and $VBN(P)$ must be decided:

- The operational frequency should be the lowest one that satisfies the performance requirement, and

- it must works with the V_{DD} and $VBN(P)$ to minimize the consumption power, thus reducing the total energy.

III. The Power Consumption Model

Microprocessors and accelerators typically consist of a core in which the switching power is dominant and memory or cache in which the leakage power is dominant. These need to be controlled independently with different $VBN(P)$, since the optimal value will be different. Although the supply voltage can be different, level shifters are needed at the boundary of the two components to transfer different signal levels. Thus, our target is that these two components be independently controlled with $VBN(P)$ and share a common V_{DD}. We represent the $VBN(P)$ for the memory part $VBN(P)M$. When both components work at the given operating frequency, the power consumption is minimized.

Here, we give the same back gate bias to nMOSFET and pMOSFET, since both transistors are commonly designed so that their characteristics are balanced. That is,

$$VBN + VBP = V_{DD}. \tag{7}$$

Hereafter, back gate voltage of the core is represented only by VBN and the memory by $VBNM$.

A. A Power Model

The leakage current increases exponentially to V_{DD} and VBN in accordance with Equations (2) and (3). That is, the leakage current to core and memory is

$$I_{leak} = I10^{AV_{DD}+BVBN}, \tag{8}$$

where I, A, and B are coefficients of exponential term, exponent part of V_{DD}, and exponent part of VBN, respectively. In the case of the memory, VBN is changed to $VBNM$. All leakage current in the chip is

$$\begin{aligned} I_{leak_{all}} &= I_{core}10^{A_{core}V_{DD}+B_{core}VBN} \\ &+ I_{mem}10^{A_{mem}V_{DD}+B_{mem}VBNM}. \end{aligned} \tag{9}$$

Here, subscript mem is given to I, A, and B for the corresponding memory part.

These coefficients vary depending on various design parameters such as critical path length of the core, memory size, and access time. It is not practical to fix them theoretically. Since the target chip already exists, the easiest way to decide them is to calculate from the measurement values of the real chip. This does not mean that our model requires measuring the target chip with all combinations of V_{DD}, VBN, and $VBNM$. On the contrary, our goal is to fix them by only a limited number of measurements, and once they are fixed, we can find the optimal V_{DD}, VBN, and $VBNM$ for a given frequency. This method can be used regardless of whether the dominant source of the leakage is subthreshold leakage current or gate tunneling current, and thus it can be used in a variety of different processes.

Unlike the leakage power, the switching power is the product of α_{at}, C, f, and V_{DD}^2 and depends not on the body bias but only on V_{DD}. Although it is possible for C to be influenced slightly by the back gate bias, we assume that it is constant. In this case, $\alpha_{at}C$ of the core and memory can be easily calculated by the increasing of the current by the operational frequency and V_{DD}.

The total current of the CPU including core and memory is represented as

$$\begin{aligned} I_{allmodel} &= I_{core} \times 10^{A_{core}V_{DD}+B_{core}VBN} \\ &+ I_{mem} \times 10^{A_{mem}V_{DD}+B_{mem}VBNM} \\ &+ (\alpha_{at}C)_{core}fV_{DD} + (\alpha_{at}C)_{mem}fV_{DD} \end{aligned} \tag{10}$$

Equation (10) calculates the power consumption with a certain clock frequency (f), and here, it must work at a required frequency f_{max}. Since the required operational frequency is shown in Equation (5), the relationship between VBN and V_{DD} that can achieve f_{max} is represented as

$$VBN = \frac{(\frac{V_{DD}f_{max}}{F})^{\frac{1}{\alpha}} - (V_{DD} - V_{t0})}{K_\gamma}. \tag{11}$$

Here, K_γ, α, and F can be known by measuring the real chip. For each module, the current is represented as

$$\begin{aligned} &I_{all_{module}} = \\ &\quad I_{module} \times 10^{A_{module}V_{DD}+B_{module}\frac{((\frac{V_{DD}f_{max}}{F})^{\frac{1}{\alpha}}-(V_{DD}-V_{t0}))}{K_\gamma}} \\ &\quad +(\alpha_{at}C)_{module}fV_{DD} \end{aligned} \tag{12}$$

Since the required frequency is the same in both modules, and the power is the sum of them, we can optimize the power consumption of the total system by finding the optimal VBN for each module with the V_{DD}.

IV. The Target micro-controller

A. V850E-Star

Here, we show an example of the proposed optimization using a real micro-controller chip. Our target is the V850E-Star [10] compatible 32-bit micro-controller for signal processing, car electronics, and digital servo motor control. It uses a RISC instruction set enhanced for application; that is, multiplication, saturation calculations, and bit manipulations are added. A 5-stage standard in-order pipeline with 46.2K gates can execute most of the instructions in a clock cycle. Considering the embedded usage, 128-Kbyte local memory modules are provided for instruction memory and data memory instead of providing a cache. The specifications of the target V850E-Star are shown in Table I. The chip was designed by several universities and companies associated with LEAP, including the authors. A photograph of the chip is shown in Figure 3. Since this chip was the first practical implementation using the 65-nm SOTB process, the core and memory use only half of the total chip.

TABLE I

IMPLEMENTATION CONDITIONS OF V850.

process	65-nm FD-SOI (LEAP SOTB)
logic gates	46.2K
local memory	128K + 128K
Logic Synthesis	Design Compiler
Routing of Layout	IC Compiler
Package	208PIN QFP
Standard Voltage	0.4V

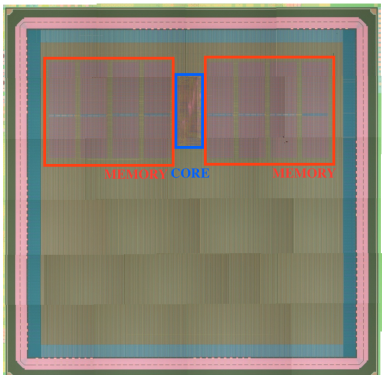

Fig. 3. Photo of implemented V850.

In this chip, independent bias and supply voltage are provided for the core and memory. Here, although we use the common V_{DD} for both parts, the power of each part can be measured separately.

B. Power consumption

Figure 4 shows the leakage power related to (a) V_{DD} and (b) VBN. Both graphs show that the leakage increases exponentially both by V_{DD} and VBN in the real micro-controller as in the proposed model. These figures also show that the memory leakage is much more than that of the core—comparing (a) and (b), it appears the leakage is more sensitive by VBN than V_{DD}. This means that the leakage can be well controlled by changing VBN. Now, let's fix the coefficients in Equation (10) from the measurement data. I_{core}, A_{core}, I_{mem}, and A_{mem} can be obtained from the relationship to V_{DD} with zero bias. We calculated the average of several measurement results and obtained the coefficients as shown in Table II. B_{core} and B_{mem} can be obtained from the relationship between the current versus VBN or $VBNM$. We also calculated the average values from several measurement results and fixed them as shown in Table II. The values for back gate bias (B) are larger than those for V_{DD}, which is a reflection of the large influence of the large memory leakage.

C. Maximum frequency

Figures 5 and 6 show the maximum operational frequency that can execute Dijkstra, a benchmark program, from the network benchmark suits of MiBench [11]. This program finds the minimum path from a source node to a destination node and includes a lot of memory accesses. Figure 5 shows the relationship to V_{DD} when zero bias is given, while Figure 6 (a) and (b) show the relationship to VBN and $VBNM$ with 0.4 V V_{DD}. Figure 5 shows that

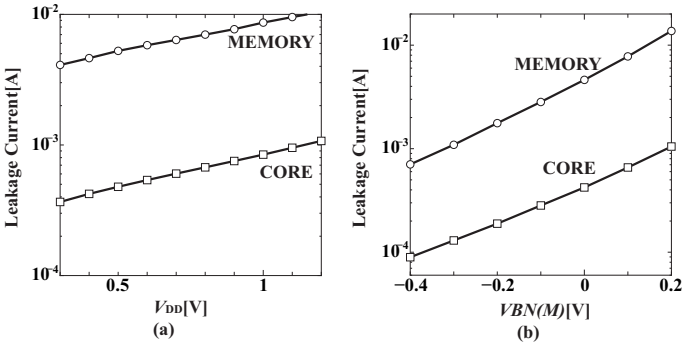

Fig. 4. Leakage current of V850: (a) characteristics of V_{DD}, (b) characteristics of VBN.

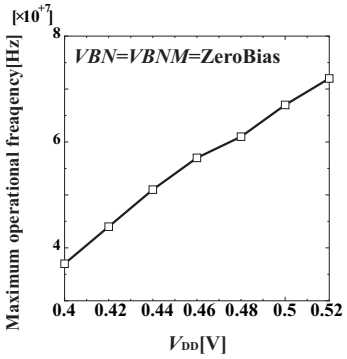

Fig. 5. Maximum frequency for V_{DD}.

the operational frequency is increased linearly to V_{DD}

From Figure 6 (a) and (b), it appears that the maximum frequency is not improved when the forward bias is given to only a part, since another part bottlenecks the whole micro-controller. In order to achieve a certain frequency, both core and memory must work at the frequency. If the counterpart is not a bottleneck, the maximum frequency also increases linearly to VBN or $VBNM$. Comparing Figures 5 and 6, it appears that the influence of V_{DD} is larger than that of VBN. Only by increasing V_{DD} by 0.1 V from 0.4 V is the operational frequency increased from 37 MHz to 67 MHz.

Now, let's fix the coefficients in Equation (11) from the evaluation results. To increase the maximum frequency linearly, α in Equation (11) must be 2. V_{t0} is given as a data sheet by the foundry. It is an average of that of nMOSFET and pMOSFET. Since the operational frequency of the microcontroller is limited by the slower part of core ($f_{maxcore}$) and memory (f_{memory}),

$$f_{max} = min(f_{maxcore}, f_{maxmem}). \tag{13}$$

Figure 6 (a) shows that the maximum frequency is proportional to the back gate bias of the core (VBN) when that for the memory ($VBNM$) is larger than 0.2 V. Also, (b) shows that the maximum frequency is proportional to $VBNM$ when VBN is larger than 0.2 V. From the slope shown in the figures, we can calculate F and $K\gamma$. These results are also shown in Table II.

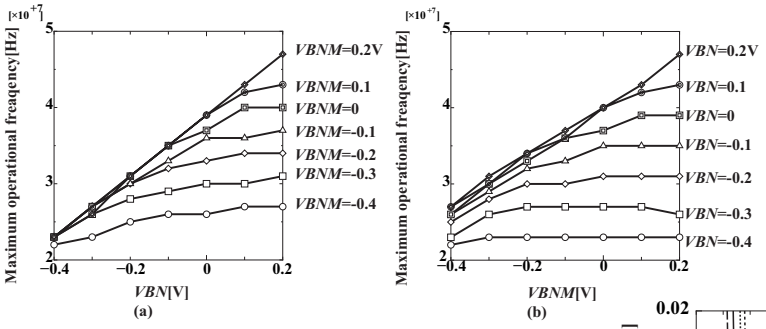

Fig. 6. Maximum frequency for VBN.

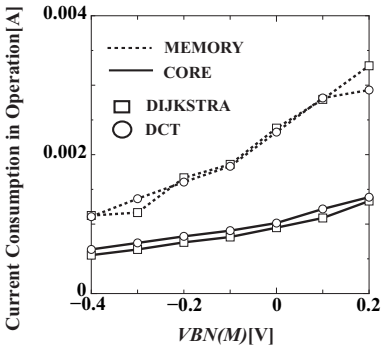

Fig. 7. Switching current with different applications.

D. Switching current

Since the switching current is influenced by the activity factor (α_{at}), it is influenced by the executed program, unlike the maximum frequency decided by the critical path of the core and access time of the memory. Figure 7 shows the current when two application programs, Dijkstra and discrete cosine transform (DCT), are executed at the maximum operational frequency. V_{DD} is fixed at 0.4 V. Unlike the memory access-centric Dijkstra, DCT includes a lot of multiply operations. However, the results show that the current difference is small. In such a small microcontroller, the switching power is mostly consumed by operations independent of the executed instructions (instruction fetch, decode, register fetch, etc.). We can therefore ignore the difference due to executed program here.

The coefficient of Equation (10) can be computed from the measured current, leakage current, operational frequency, and V_{DD}. The results for the core and memory are shown in Table II.

V. Finding optimal V_{DD}, VBN and $VBNM$

Now, we have all the parameters for finding the optimal voltage setting. For a given frequency, VBN can be computed from Equation (11). By replacing VBN in Equation (10) with the obtained value, we can draw a graph for the minimum power consumption to V_{DD}, as shown in Figure 8. V_{DD}, VBN, and $VBNM$ for the minimum point in the graph are shown in Table III. These are the optimal voltage settings to achieve the required operational frequency. As expected, the power consumption was reduced as V_{DD} was decreased to the minimum voltage but rapidly increased due to the leakage current increased by

TABLE II
Coefficient of Equation (10).

	CORE	MEM
I	2.5876×10^{-4}	3.0523×10^{-3}
A	0.51921	0.45172
B	1.7926	2.1563
F	6.6641×10^{8}	6.8350×10^{8}
$K\gamma$	8.2874×10^{-2}	6.1342×10^{-2}
$\alpha_{at}C$	6.2478×10^{-11}	1.3669×10^{-10}

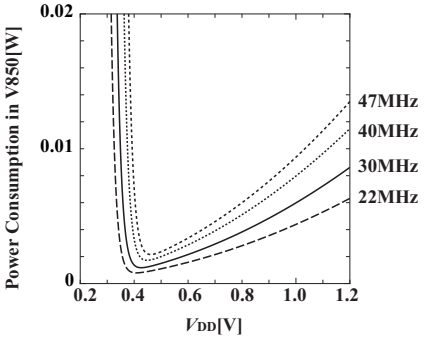

Fig. 8. Power of V850 by calculating Equation (10).

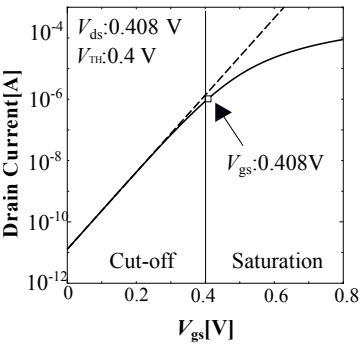

Fig. 9. I_D-V_{gs} characteristics.

the forward bias needed to achieve the required operational frequency. The minimum point was increased when the required operational frequency was increased. Table III shows that the reverse bias is needed for both the core and the memory to minimize the power. For the memory, a larger reverse bias is needed, reflecting its larger leakage power. The optimal VBN and $VBNM$ are increased for a higher target frequency since the ratio of leakage current and switching current is changed by the operational frequency.

A. Accuracy of the optimization

Since the proposed model is based on α-power low, it must be ascertained whether MOSFETs operate on over threshold region at calculated voltage or not. Figure 9 shows $\log(I_d)$-V_{gs} characteristics of nMOSFET in SPICE simulation on -0.7565V of reverse bias and 0.408V of supply voltage, which is lowest V_{DD} and highest V_{TH} in Table III. A straight line is an extentension which has the same slope of sub-threshold region of the MOSFET. Here, from $V_{gs} = 0.408$, $\log(I_d)$-V_{gs}, the curve begins to turn away from the straight line. This shows MOSFETs do not have exponential characteristics in V_{DD}=0.408V. Over threshold region of a MOSFET means that V_{gs} is higher than V_{TH}, and the calculated results satisfy this condition. With -0.7565V of reverse bias, V_{TH} is 0.400 in SPICE simulation. Therefore, 0.408V of V_{DD} is higher than V_{TH}.

The values in Table III obtained from the expressions include a few errors due to the approximation. In order to determine the accuracy of the optimization from the expressions, we investigated the minimum power by measuring the real chip with various V_{DD}, VBN, and $VBNM$. Note that this brute force search required plenty of time. The values obtained with this search are also listed in Table III. It shows that the error is 50 mV at maximum. Ta-

TABLE III

Error between calculated value and measured value (voltage)[V].

Frequency	Calclulated value	Measured value
22MHz	$V_{DD} = 0.408$	$V_{DD} = 0.444$
	$VBN = -0.5423$	$VBN = -0.535$
	$VBNM = -0.7565$	$VBNM = -0.753$
30MHz	$V_{DD} = 0.426$	$V_{DD} = 0.463$
	$VBN = -0.4889$	$VBN = -0.485$
	$VBNM = -0.68895$	$VBNM = -0.682$
40MHz	$V_{DD} = 0.448$	$V_{DD} = 0.492$
	$VBN = -0.4467$	$VBN = -0.446$
	$VBNM = -0.6371$	$VBNM = -0.633$
47MHz	$V_{DD} = 0.462$	$V_{DD} = 0.512$
	$VBN = -0.4162$	$VBN = -0.416$
	$VBNM = -0.5993$	$VBNM = -0.604$

TABLE IV

Difference between calculated value and measured value (power)[mW].

Frequency	Calclulated value	Measured value (The difference from model)
22MHz	0.7932	0.9072(12.6%)
30MHz	1.176	1.308(10.1%)
40MHz	1.725	1.554(11.3%)
47MHz	2.154	2.047(5.23%)

ble IV compares the power consumption when values from the expressions and the brute force search are applied. It shows that the difference is less than 12.6%. Considering the time for measurement, our model is an efficient means of finding the optimized setting.

B. Power reduction by the optimization

Figure 10 shows the power consumption when the optimized setting is used and only VBN is optimized with 0.4 V fixed V_{DD}. For all target frequencies, the optimized setting reduced the power consumption. Since 0.4 V is suitable for the lower frequency, the difference is large for 47 MHz. About 73% of power can be saved by using the optimization. Even for 22 MHz, the optimized setting achieved a power reduction of about 7%. This demonstrates that the optimization for three voltages works efficiently.

VI. **Conclusion**

We proposed a method for finding the optimal combination of supply voltage and body bias voltage to the core and memory and applied it to a real micro-controller chip using SOTB CMOS technology. By obtaining several coefficients of equations for leakage power, switching power, and operational frequency from the real chip measurements, we were able to obtain the optimized voltage setting for the target operational frequency. The power consumption lost by optimization errors was 12.6% at maximum, and we could save at most 73.1% of power in the case where only the back gate bias is optimized in fixed V_{DD}. This method can be applied to the latest FD-SOI technologies. In this study, we ignored the influence of GIDL, since it is commonly dominant when a large V_{DD} and strong reverse bias

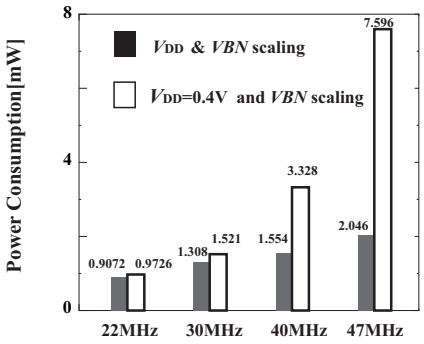

Fig. 10. A comparison of power consumption.

are given—that is, in cases far from the optimized point. The treatment of this influence is our future work. Also, we did not consider the temperature and variances of the chip. Since the target micro-controller must work with the required frequency in any case, we also intend to set some control margins.

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