Time Analysis of Applying Back Gate Bias for Reconfigurable Architectures with SOTB MOSFET

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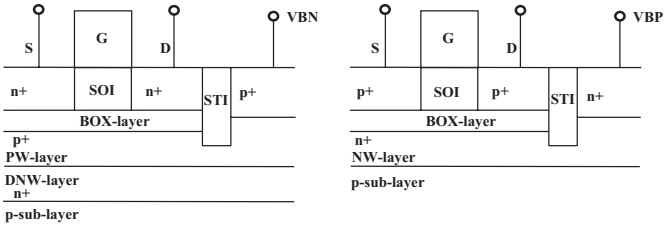
Abstract - Response time of the dynamic back gate bias scaling of large scale digital modules implemented with silicon on thin BOX (SOTB) technology developed by LEAP was analyzed using real chips. A reconfigurable accelerator cool mega array (CMA) and two different prototypes of microcontroller V850 E-star were utilized for the measurement. Evaluation results revealed that the response time is related to the chip area which shares the bias voltage rather than the leakage current itself. The leakage current can be mostly stable 180.0us and 270.2us after changing bias voltage of CMA and V850E-Star, respectively. The possibility of the dynamic back gate bias scaling within milliseconds for dynamic reconfigurable architectures was shown.

I. Introduction

Extremely low energy computation has been required for sensor networks, ware-able systems and cyber-physical systems. Near threshold level devices which work with extremely low power supply have been used for such purposes, but their performance is not always enough for recent sophisticated applications[1].

Silicon On Thin Box (SOTB) MOSFET has been developed to support enough high performance with low supply voltage [2]. It can control the threshold level by changing the back gate bias. Leakage current can be decreased by applying a back gate bias to a reverse direction (reverse bias), while the delay time is increased. On the other hand, operational speed can be increased by allowing the increase of leakage current by the forward bias. Appropriate balance of performance and power consumption can be selected for each application by setting the back gate bias voltage. By separating back gate bias to multiple components of the system and controlling them independently, we can optimize the performance and energy more precisely. We have tried to apply this technique for microcontroller and PE-Array of a coarse grained Reconfigurable Accelerator CMA-SOTB [3], and a core and a memory of an embedded microcontroller V850[4].

These studies have assumed that the processing starts enough time after setting the bias voltage. However, it is necessary to know how much time is needed for responding the chip by changing the back gate bias. For example, in sensor network systems, the leakage current can be suppressed to extremely low level with strong reverse bias voltage in the stand-by mode. When an event occurs, it must wake up by change the back gate bias to the normal voltage and start the computation. If the response time for the back gate bias is too long, the node might miss the time for measurement. However, there has been no report of the response time for the back gate bias of SOTB chips.



(a) **(b)**

Fig1. Structure of SOTB MOSFET (a)nMOS(b)pMOS

Here, we measure such response time by using an off-chip generator, and investigate the relationship between the target chip area.

The paper is organized as follows: Section II provides methods of time analysis of applying back gate bias. Section III explains detail of experiment and how to do. Section IV shows and considers results of experiment. Finally, we present the conclusion in section V.

II. Back Gate Bias

A. Change of the threshold voltage

Fig.1 depicts the crosscutting structure of SOTB MOSFET. SOTB MOSFET is a kind of FD-SOI and a transistor is formed on the ultra thin Box layer. A triple-well structure is also adopted, so that the back gate bias can be applied to every well adaptively, and V_{th} can be well controlled.

V_{th} of a MOSFET is the gate voltage that the depletion layer of the transistor is maximized, and the maximum depletion layer width of FD-SOI is depending on the thickness of the SOI layer of the transistor [5]. The voltage of back gate bias VBN given to nMOSFET influences as follows.

- Positive electric charge increases in the well and negative electric charge increases in SOI at the VBN > 0, and depletion layer becomes easy to be formed in SOI. Therefore, V_{th} is decreased (forward bias).
- Positive electric charge increases in SOI and negative electric charge increases in well at VBN < 0, and depletion

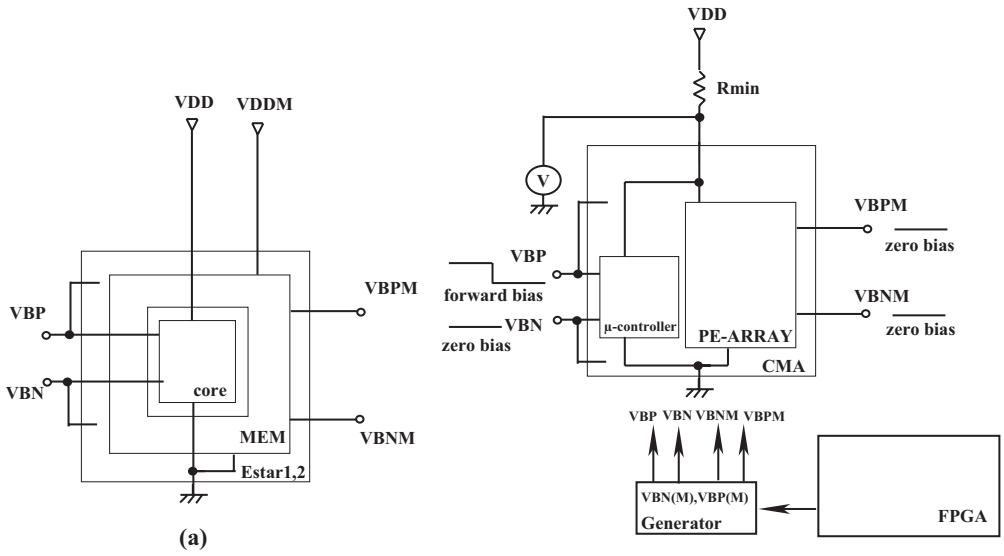


Fig3. Diagram of experiment conditions

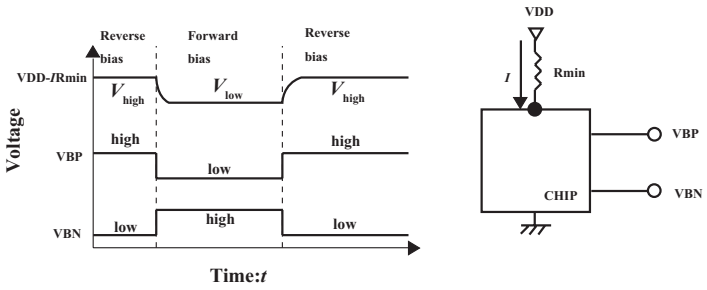


Fig2. Expected waveform of experiment

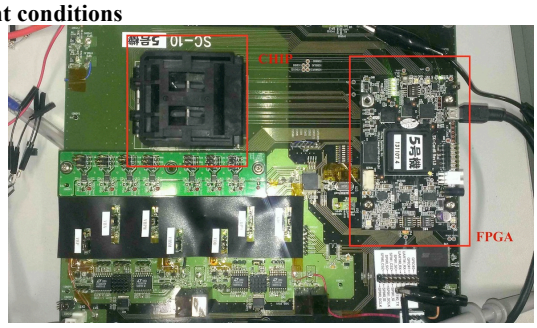


Fig4. Picture of experiment conditions

layer becomes hard to be formed in SOI. Therefore, V_{th} is increased (reverse bias).

Here, VBN=0V is called zero bias.

On the contrary, the body bias to pMOSFET, VBP works according to the difference from the supply voltage (V_{sp}),

・Positive electric charge increases in well and negative electric charge increases in SOI at the VBP > V_{sp}, and depletion layer becomes hard to be formed in SOI. Therefore, V_{th} is increased (reverse bias).

・Positive electric charge increases in SOI and negative electric charge increases in well, when VBP < V_{sp} , and depletion layer becomes easy to be formed in SOI. Therefore, V_{th} is decreased (forward bias).

Here, zero bias is the case when VBP=VDD.

When V_{th} decreases (forward bias), the leakage current (I_{leak}) of MOSFET increases, and the delay time decreases. When V_{th} increases (reverse bias), I_{leak} decreases but the delay time increases. In other words, we can find the trade-off by controlling back gate bias adaptively for a given purpose of the architecture.

B. The response time of applying back gate bias

After applying back gate bias, it is necessary to know how much time is needed to express effect of back gate bias in a chip. Because of the capacitance to the well and resistance for the wiring to the back gate of SOTB MOSFET, a certain delay is required until back gate bias voltage works its effect. Generally when back gate bias is applied in the MOSFET, I_{leak} changes by its value. Here, we measure the response time of back gate bias by monitoring I_{leak} flowing from the power supply (VDD) to the chip. In order to monitor I_{leak}, resistance enough small compared with the chip resistance is provided between chip and VDD. A fall time and rise time at resistance represents the change of leakage current. Fig.2 shows recorded waveforms by the experiment. When the waveform becomes stable, the back gate becomes the steady state. Here, we define the response time of the back gate bias as the rise up time and fall down time of the waveform. That is, the change from 10% to 90% of V_{high} is referred as t_r, while from 90% to 10% is t_f.

When we use devices under the severe condition, some margin should be added to the above response time. Thus, we define the response time with margin t_{rm} as follows.

t_{rm}: The time from 0% to 90%

t_{fm}: The time from 100% to 10%.

Ⅲ. Experiment

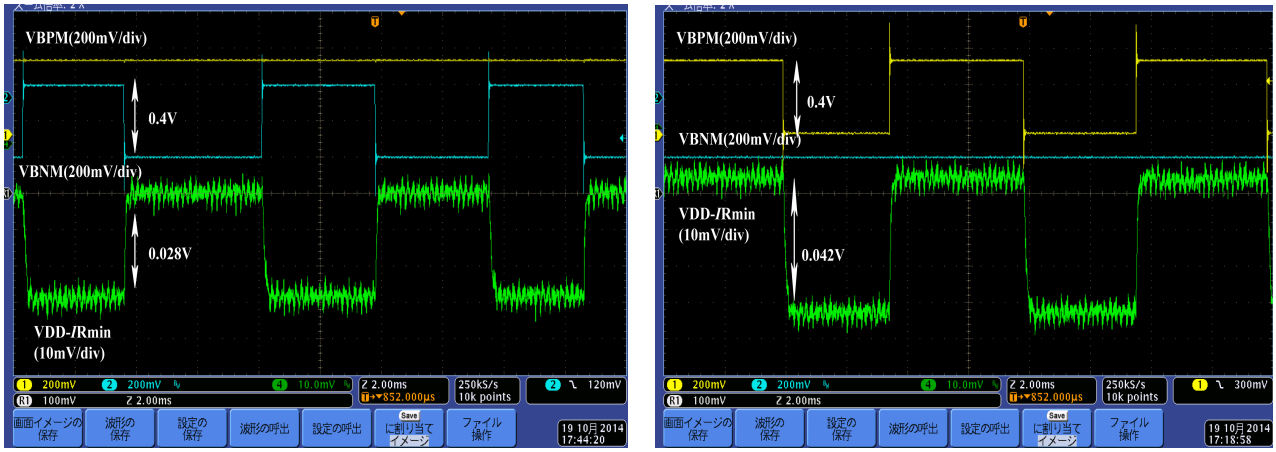
Fig.3 shows diagram of the experimental system, and Fig4 shows a photo of it. We used 3 real chips. Two are different

Table1. Area of macro

	Area [μm^2]
Estar1	SRAM:5.8×10^6 core:1.6×10^5
Estar2	SRAM:1.3×10^6 core:1.7×10^5
CMA	PE-ARRAY:4.2×10^6、μ-con2.0×10^6

Table2. Summary of experiment condition

Process	LEAP65nm
Package	208PIN QFP
Routing of Layout	Design Compiler
Standard power supply	0.4V
Oscilloscope	DPO4104
Back gate bias	0.4V(forward)



(a) (b)

Fig5. Experiment results of PE-ARRAY (a)Pulse applied to VBNM(b)Pulse applied to VBPM

prototypes of microcontroller V850E-star, and consist of SRAM macro (MEM) and microcontroller core macro that executes instructions (core). From now on, we call two V850 chips Estar1 and Estar2. Estar1 has an instruction and data memory module on chip. Estar2 has only data memory on chip. Thus, a macro area of them is different from each other. In Estar1 and Estar2, power supply (VDD and VSS), and back gate bias(VBN(M), and VBP(M)) are connected to each macro independently as shown in Fig3.(a). VBN and VBP connected to a core macro are also connected to well of the whole chip except MEM macros. The third chip is a reconfigurable accelerator cool mega array (CMA). CMA consists of PE-ARRAY macro for computation and microcontroller macro that controls the data management between memory and PE-ARRAY. The back gate bias (VBP(M) and VBN(M)) is applied each macro individually, and the VDD wiring is shared with the microcontroller macro and PE-ARRAY macro. In CMA, VBP and VBN are not only connected to the microcontroller macro, but also connected to the well of the whole chip except PE-ARRAY macro like Estar1 and Estar2. Table1. shows area of each macro.

Here, the tool used for the layout is Synopsys IC Compiler, and the global wiring of VBP(M) and VBN(M) to macro forms a mesh structure. Applying back gate bias is performed by VBP(M) and VBN(M) generator that is controlled by an FPGA. Here, one of two macros in the chip is given a pulse signal for back gate bias, the other macro sets it in a zero bias state. With the limitation of the analysis system, only one of bias voltages can be changed. Thus, one of VBP(M) or VBN(M) is fixed zero bias, and the other is applied of pulse as shown in Fig3.(b). The pulse generator and power supply are implemented with emitter-follower transistor, and output impedance is enough low. Rmin for current monitors is changed by each target macro. Since I_{leak} varies according to a circuit, by changing Rmin, excessive voltage descent of VDD can be prevented at the time of the large I_{leak} macro analysis. We set Rmin so that voltage descents by Rmin did not exceed 0.05V this time.

The information about chip implementation is summarized in Table 2. The process used for the chip implementation is LEAP 65nm SOTB process, and the standard power supply voltage is VDD=0.4V. The package of the chip uses 208PIN QFP and an oscilloscope DPO4104 is used for wave pattern indication.

The back gate bias gives 0.4V from zero bias at the time of t_f analysis in the forward direction and goes back up in zero bias from the voltage of the forward bias at the time of the t_r analysis.

IV. Results

A. A response time of applying back gate bias

Fig.5 shows waveforms observed in the experiment. They were obtained by giving forward bias pulses (0.4V) to (a)VBNM and (b)VBPM of PE-ARRAY of the CMA. In three waveforms, the top is VBPM, the next is VBNM, and the bottom is the change of leakage current measured by

Table3. Time of applying back gate bias (no margin)[μs] (I_{leak}[mA])

		Estar1		Estar2		CMA	
Pulse:VBP(M) Zero bias:VBN(M)		MEM (9.62)	core (0.457)	MEM (0.199)	core (0.998)	PE-ARRAY (3.46)	μ-controller (1.78)
	t_r	80.99(27.1)	219.7(1.90)	96.68(0.851)	120.8(1.31)	91.15(12.5)	103.6(10.2)
	t_f	118.5(27.1)	229.3(1.90)	62.88(0.851)	78.76(1.31)	125.2(12.5)	160.8(10.2)
Pulse:VBN(M) Zero bias:VBP(M)	t_r	98.67(16.0)	191.5(1.05)	75.68(0.437)	101.8(1.27)	84.55(10.7)	80.89(8.62)
	t_f	170.1(16.0)	210.9(1.05)	69.30(0.437)	119.9(1.27)	129.9(10.7)	115.3(8.62)

Table4. Time of applying back gate bias (added margin)[μs]

		Estar1		Estar2		CMA	
Pulse:VBP(M) Zero bias:VBN(M)		MEM	core	MEM	core	PE-ARRAY	μ-controller
	t_{rm}	94.71	248.7	109.0	122.2	99.09	114.7
	t_{fm}	160.5	270.2	64.27	80.24	148.7	183.0
Pulse:VBN(M) Zero bias:VBP(M)	t_{rm}	115.1	208.3	92.64	121.8	96.72	92.73
	t_{fm}	180.9	257.4	82.54	105.0	167.0μs	135.7

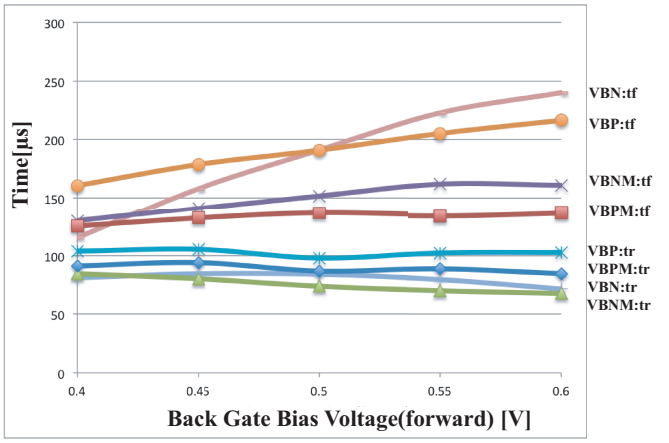


Fig6. t_r t_f vs voltage of back gate bias

VDD-*I*Rmin. The range of the oscilloscope is 200mV/div in VBPM and VBNM, and 10mV VDD-*I*Rmin, respectively. Here, the voltage drop of Rmin by I_{leak} is held down 0.028V and influence of Rmin is very low.

Here, t_r is the case when the forward bias is changed into the zero bias, while t_f is corresponding to the case when the forward bias is given.

From Fig.5(a), we can read that t_r of VDD-*I*Rmin is 84.55μs, t_f is 129.9μs. t_{rm} is 96.73μs, and t_{fm} is 167.0μs, respectively.

The difference between t_{fm} and t_f is 37.1μs. It shows that the time from 90% to 100% is relatively large, and we need to wait about additional 30% time if we must wait for the complete stable state.

Table3 and Table4 show response time of three chips measured by the same way as Fig.5. Table 3 shows the back gate bias without a margin, and Table 4 shows with it. The numbers in the parenthesis in Table 3 show the absolute value of leakage current (I_{leak}).

Table 3 and Table 4 show that the response time of VBN and VBP is not the same for the same module. First, let's focus on t_r. In most cases, the response time of VBP is 10%-20% longer than that of VBN. Exception is MEM of Estar1 whose response time of VBN is slightly longer than that of MEM. About t_f, there is no tendency observed. In a module (for example, the core of Estar1), response time of VBP is larger than that of VBN, but the opposite relationship can be observed in the core of Estar2.

When $t_r > t_f$ in VBP, the same relationship can be observed in VBN. The exception of this rule is core of Estar2, but including the margin, in Table 4, this relationship can be observed for all figures. About the relationship between leakage current and module area will be discussed later. Fig.7 represents table3. in figures, and we can see this situation.

Table4. shows that according to the target hardware modules, response time varies from 122.2μs to 270.2μs. We can use dynamic control of back gate bias if the application allows this range of response time.

B. Voltage characteristics of back gate bias

Fig.6 shows relations between response time of back gate bias and the voltage of back gate bias. The vertical axis shows t_r, and t_f, while the horizontal axis is voltage of the forward bias (0.4V~0.6V). The evaluated chip is CMA. This graph shows that the response time is almost constant for the back gate bias voltage when the forward bias is changed to zero bias (t_r). However, when the zero bias is changed to forward bias (t_f), the response time is slightly increased. This is bad news for dynamic back gate bias scaling, since the wake-up time is increased depending on the forward bias voltage value. Fortunately, the change is not so large especially in the range of reasonable forward bias.

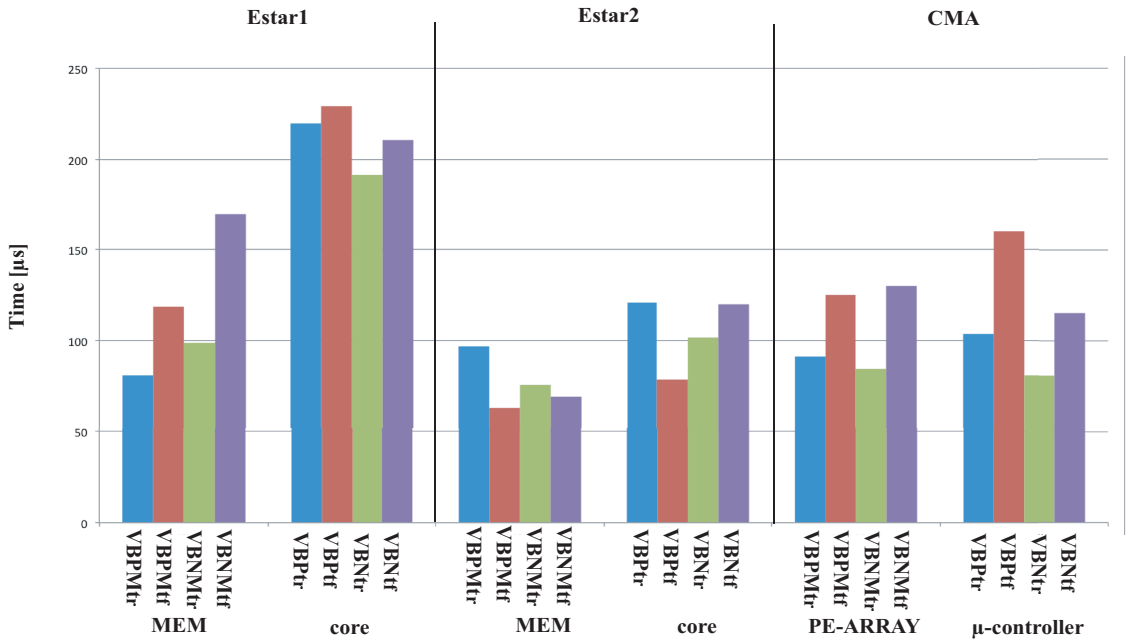


Fig7. Applying time of back gate bias in Table3.

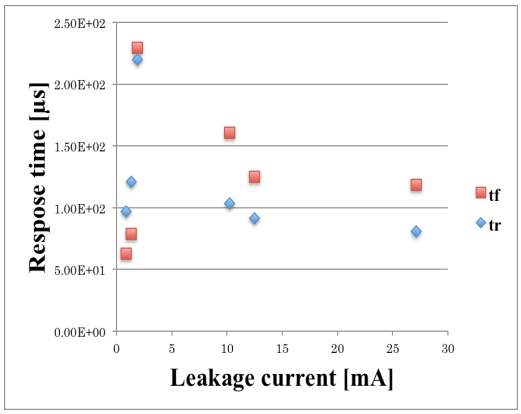


Fig8. The correlation diagram between response time and leakage current

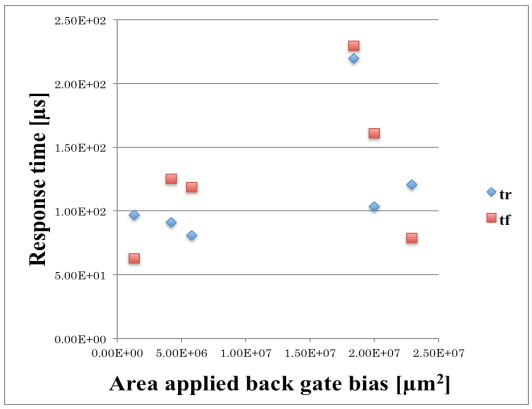


Fig9. The correlation diagram between response time and Area applied back gate bias

C. Response time vs. leakage current

Leakage current I_{leak} is proportional to the cell area which actively operates. Fig. 8 shows the correlation diagram between response time and leakage current. This diagram shows there is almost no relationship between them. Since I_{leak} comes from power supply (VDD), it might be no relationship the response time of the back gate bias.

D. Leakage current vs. core area

The area of active cells is not related to the leakage current. However, the core area is not equal to the active cell area in the real chip implementation. If there is area not used in the chip, it must be filled with filler cells which share the same back gate bias. As shown in Fig.3, the back gate bias connected to the core macros (core in Estar1 and Estar2, and microcontroller in CMA) are also connected unused area of the chip. Thus, the total area to which back gate bias is delivered becomes larger than the core area itself. Here, we refer the total area where back gate bias is delivered as core area.

Fig.9 shows the correlation diagram between response time and core area. This time, the response time of smaller core area is small. But, the relationship is not so apparent. The response time of Estar1 core is much larger than others.

More numbers of evaluation are required to find the relationship between leakage current and core area.

V. Summary and Conclusions

We evaluated time applying back gate bias to a chip using 65nm SOTB CMOS process with the off chip bias generators, and analyzed it. From the viewpoint of dynamic back gate

bias scaling, the following results were observed.

(1) The response time of VBP is mostly larger than that of VBN when forward bias is removed. That is, the sleep-down transition. Since both voltages are changed simultaneously, we must focus on VBP.
(2) The time for sleep-down (t_r) and wake-up (t_f) have the same tendency for each hardware module, although in some modules, tr<tf but the opposite relationship is observed in other modules.
(3) The time for sleep-down is almost independent from the bias voltage, but wake-up response time is slightly increased with the forward bias voltage.
(4) There is almost no relationship between the response time and leakage current of the target hardware module.
(5) If the core area which share the back gate bias is large, the response time becomes large. However, the relationship is not so apparent.

Since the response time of all modules is less than 300us including the margin, we can use dynamic back gate if application allows this delay.

This research includes the first measurement of the response time of back gate bias for SOTB real chips, and the experiments are not enough. We must measure more numbers of chips and establish theoretical bases for analysis.

Acknowledgements

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