CAUI-4 Application Requirements

IEEE 100GNGOPTX Study Group

Ali Ghiasi

Broadcom Corporation

July 17, 2012

San Diego

List of Suporters

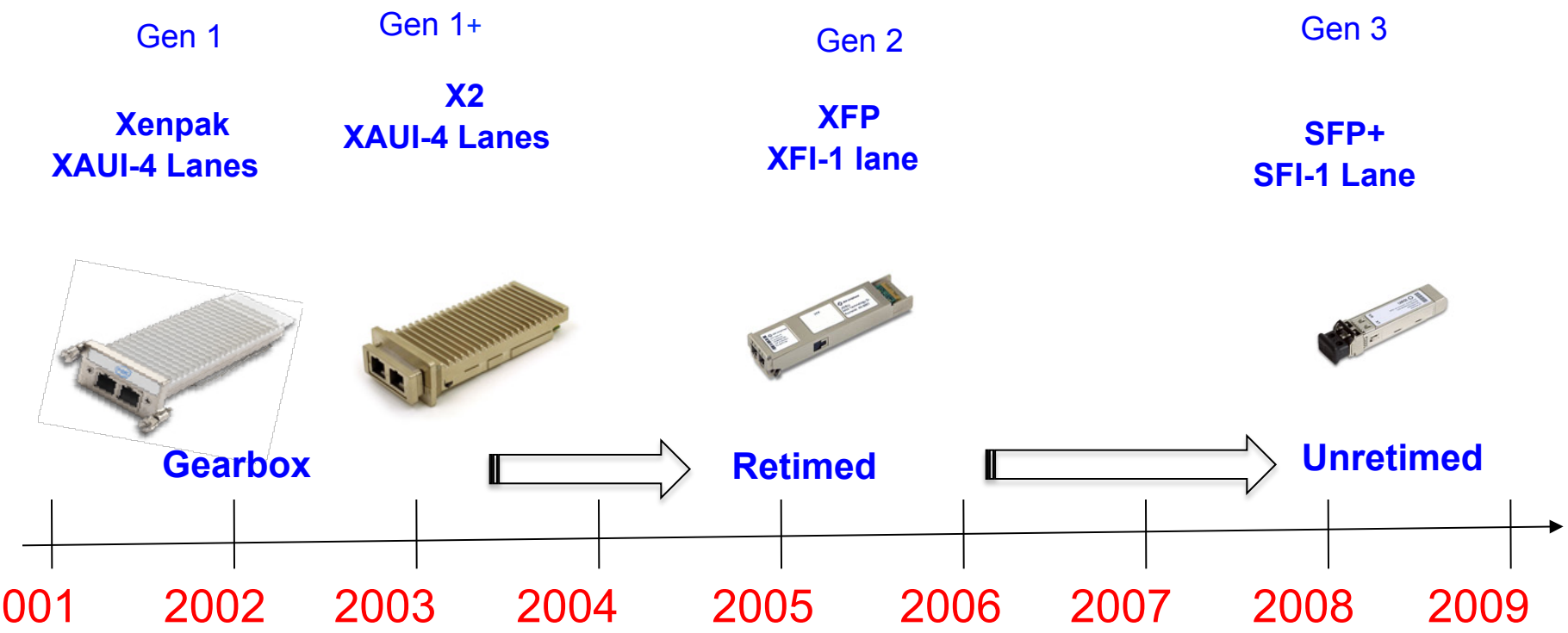
- Mike Li – Altera
- Vasu Parthasrathy - Broadcom
- Richard Mellitz – Intel
- Ken Lusted – Intel
- David Chalupsky – Intel

Overview

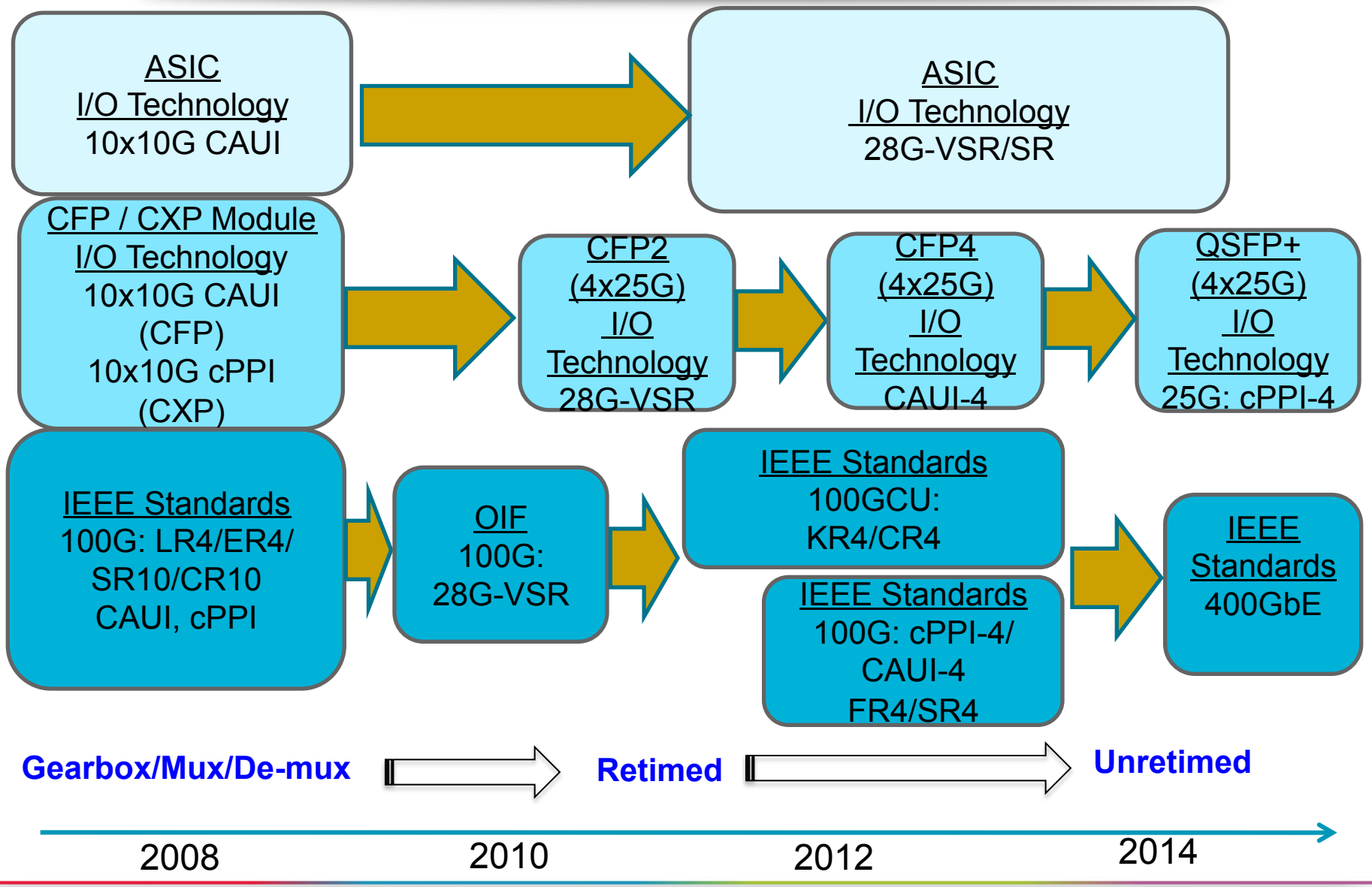
- Alphabet soup
- 100 GbE I/O trend
- 10G CAUI application model
- Line card requirement
- Architectural implementation
- PCB reach
- Proposed CAUI-4
- Impact of CAUI-4 with higher loss budget

10 GbE Alphabet Soup

- We will be very lucky if 100 GbE can follow the same alphabet
  - CFP is 100 GbE equivalent Gen 1 (Xenpak)
    - CFP2 is 100 GbE equivalent Gen 1+ (XPAK)
    - CFP4 100 GbE equivalent Gen 2 (XFP)
    - QSFP28 100 GbE equivalent of Gen3 (SFP+)



100GbE I/O Trends



Reality Check and Market Requirement

- There is a clear need to define next generation chip to chip and chip to module interface CAUI-4 in 100GNGOPTX project
  - 10G CAUI had loss budget of 10.5 dB from chip to chip at Nyquist or 7.9 dB allocated to the host sufficient to support 8-16” PCB depending on the material
- OIF 28G-VSR is defined for chip to module applications where a gearbox is placed 100 mm away from the module
  - When the gearbox is integrated into the large switch ASIC then OIF 28G-VSR does not meet the reach requirement
- 100GNGOPTX project focus is development of PMDs and there is little interest to define more complex unretime cPPI-4 at this point
  - SFP+ took more than 3 years of development in a dedicated group but its fruit enabled definition of 40G/100G PPI interface in 802.3ba
- CAUI-4 interface will be more in line with OIF 28G-MR loss budget of 20 dB and need to support support
  - 250 mm of host PCB in chip to module applications with one connector
  - 300 mm of host PCB in chip to chip applications with one connector

10G CAUI Application Reference Diagrams

- 10G CAUI has 10.5 dB of loss at 5.15625 GHz supporting 250 mm of PCB
  - CL83A define chip to chip application
  - CL83B define chip to module application

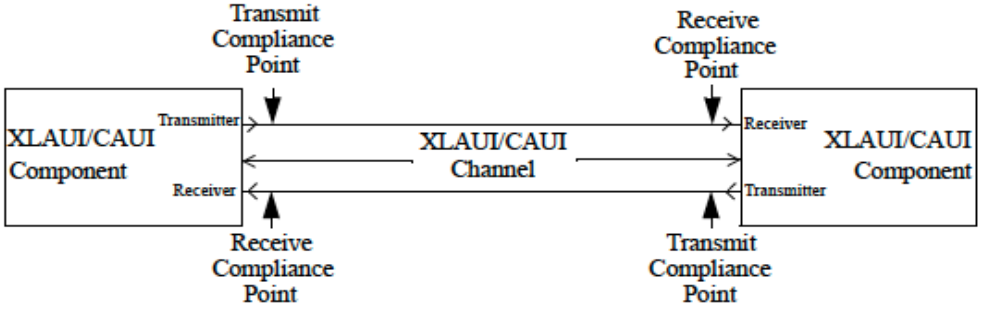


Figure 83A–2—Definition of transmit and receive compliance points

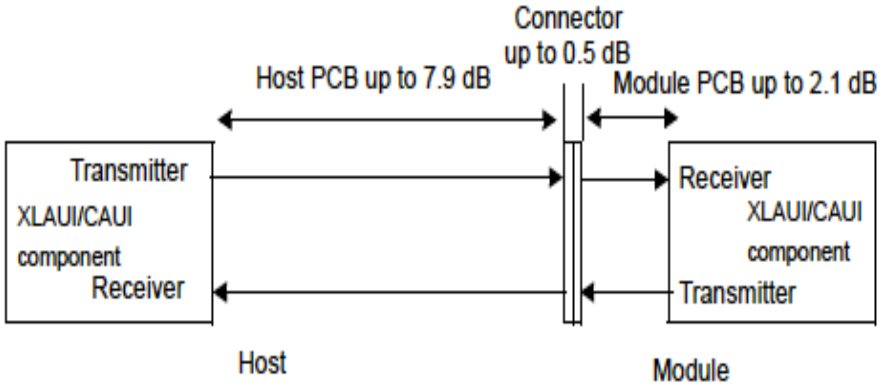
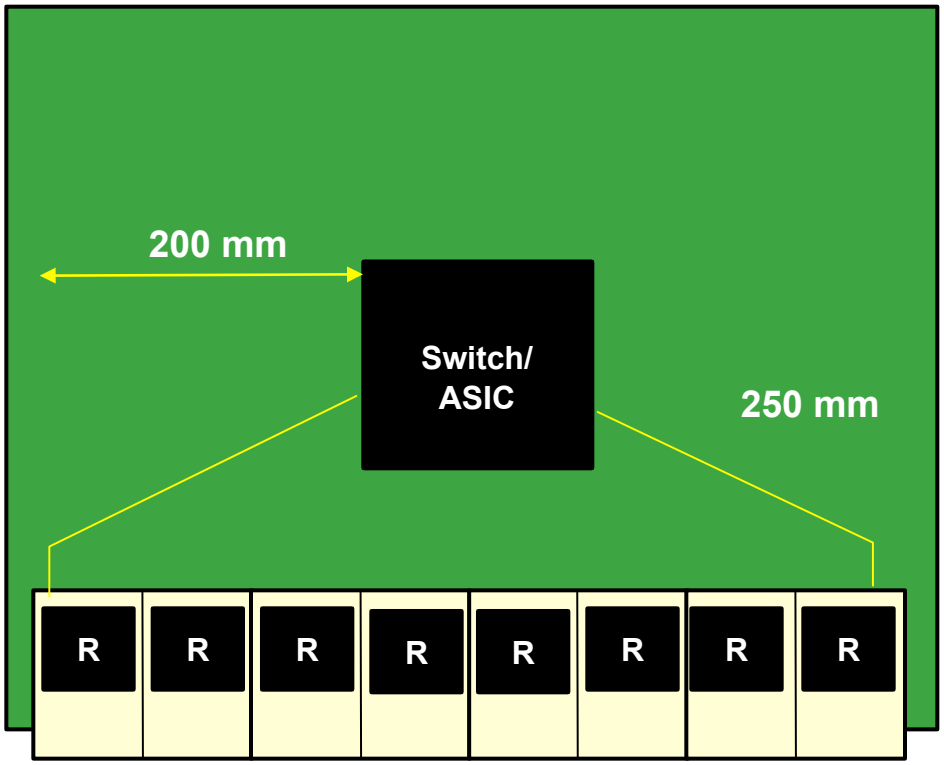
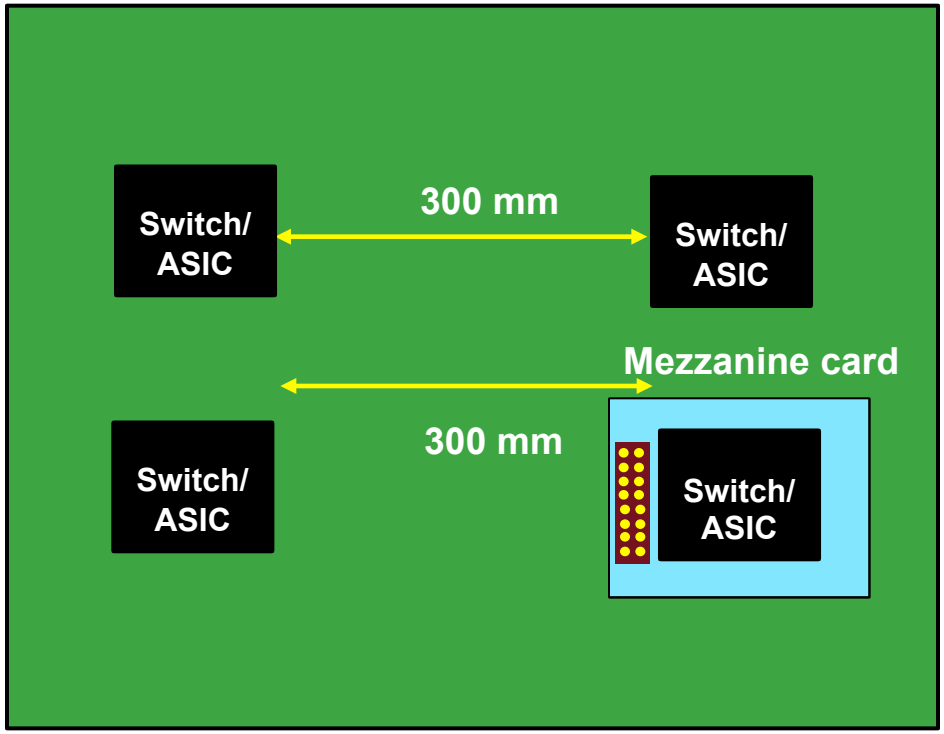


Figure 83B–2—Chip-module loss budget at 5.15625 GHz

CAUI-4 Applications

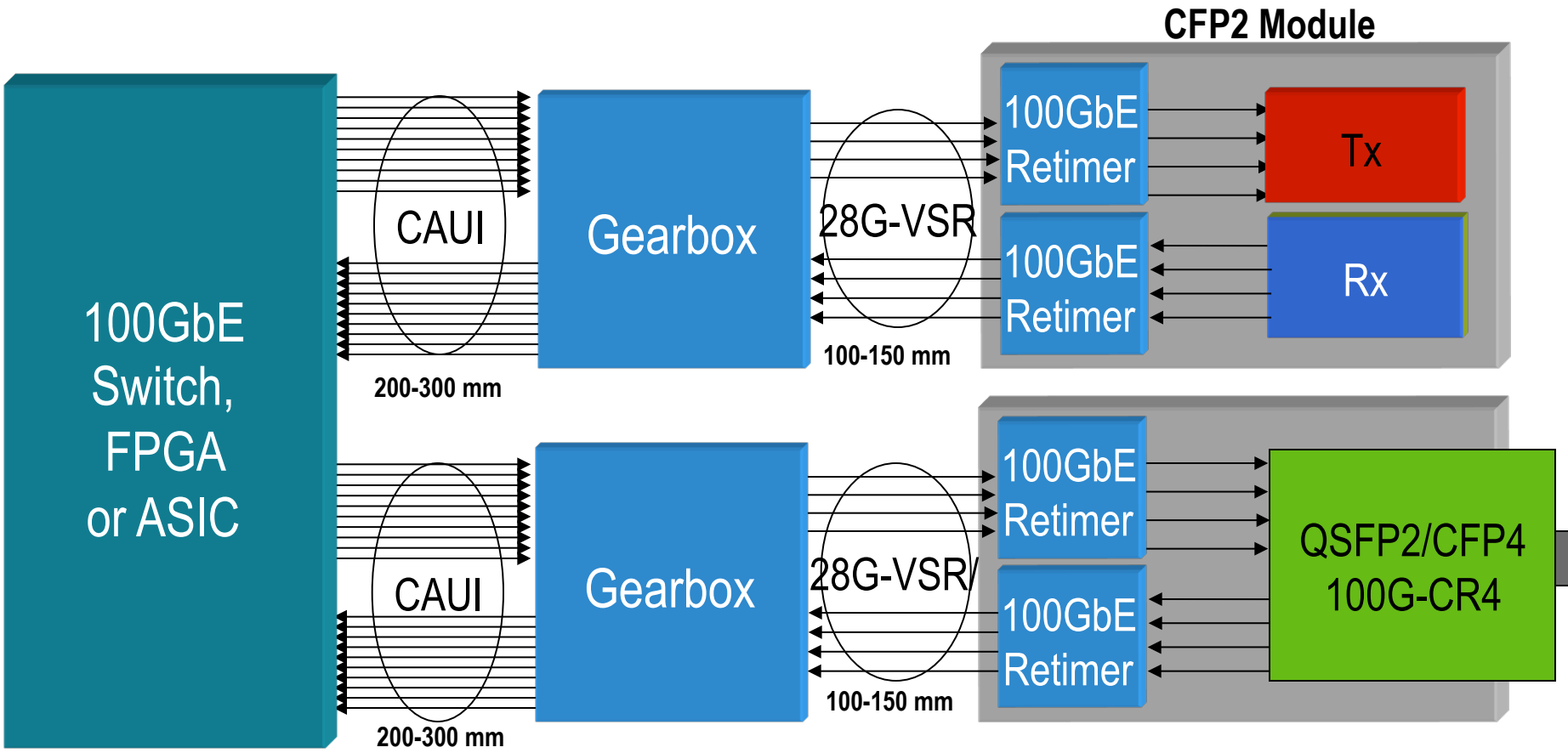
- Chip to module applications supporting 250 mm
- Chip to chip applications supporting 300 mm





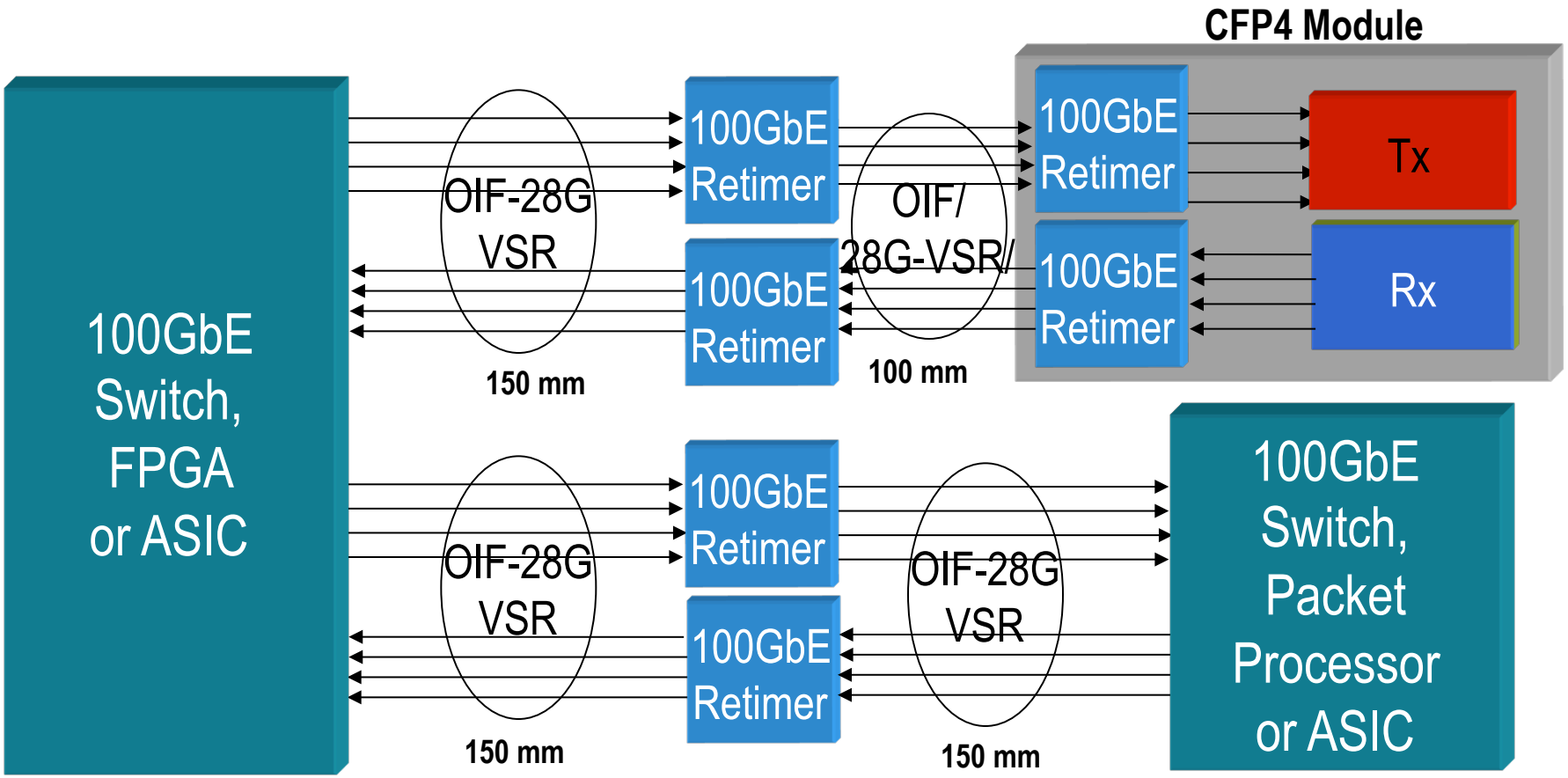
Current Retimed Applications with "CFP2"

- CFP2 is retimed interfaced works nicely with current silicon generation where Gearbox is placed 100 mm away from module



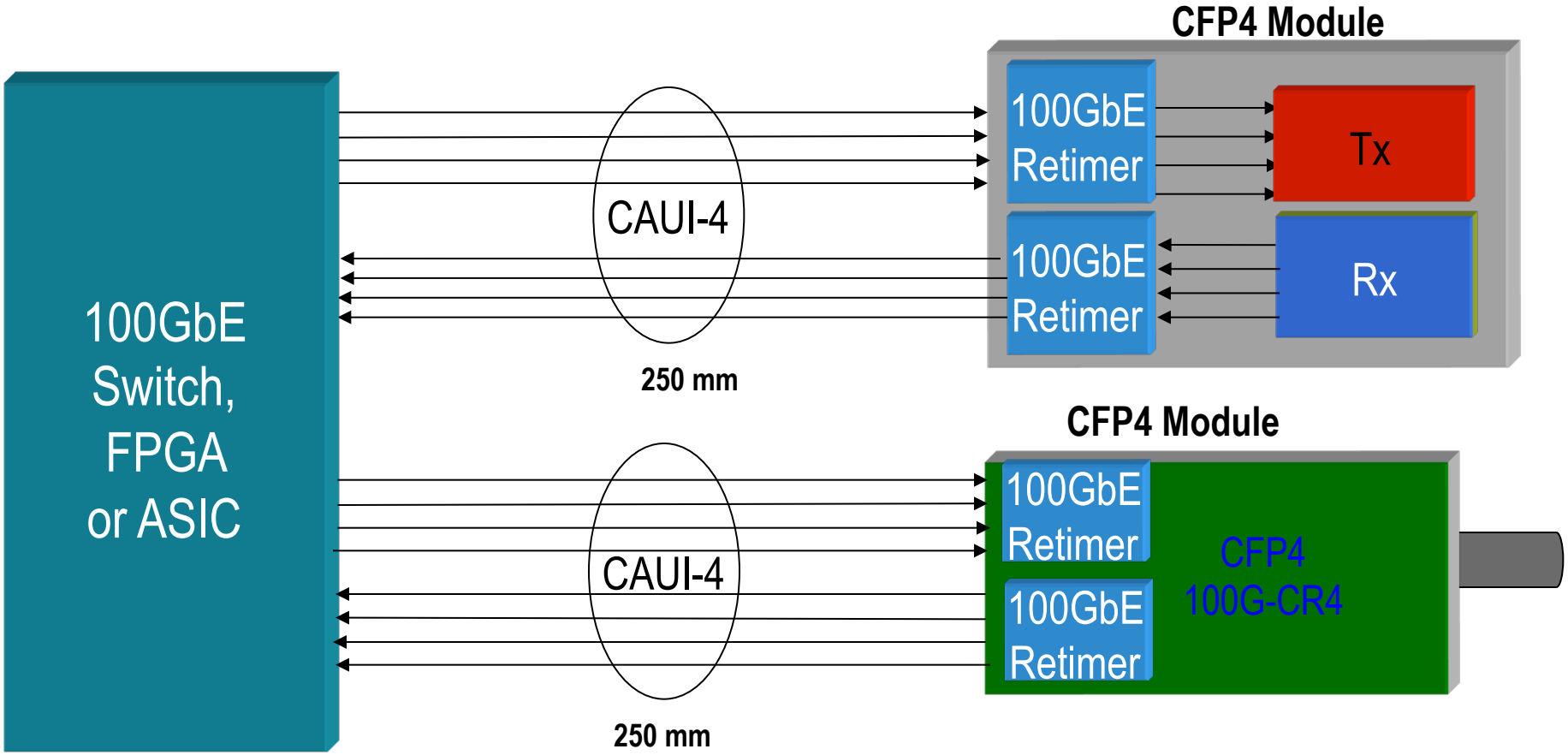
Sub-Optimum Retime Implementation

- If CAUI-4 loss budget is only 10 dB most switch/ASIC would require mid-span retimer!
  - 10G CAUI met these application without mid-span retimer



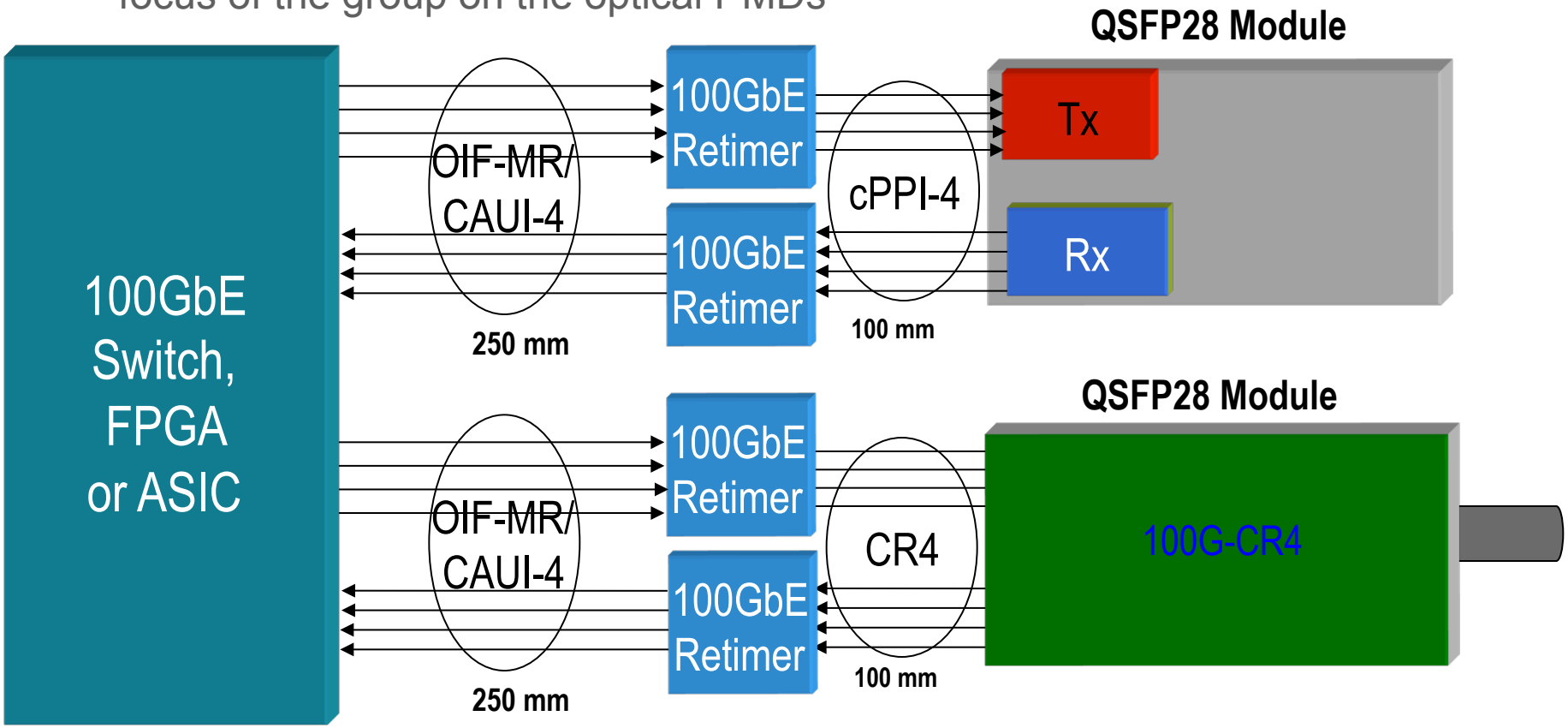
CAUI-4 Chip to Module Application Reference Model

- CAUI-4 must support equivalent reach of the 10G CAUI which was 250 mm



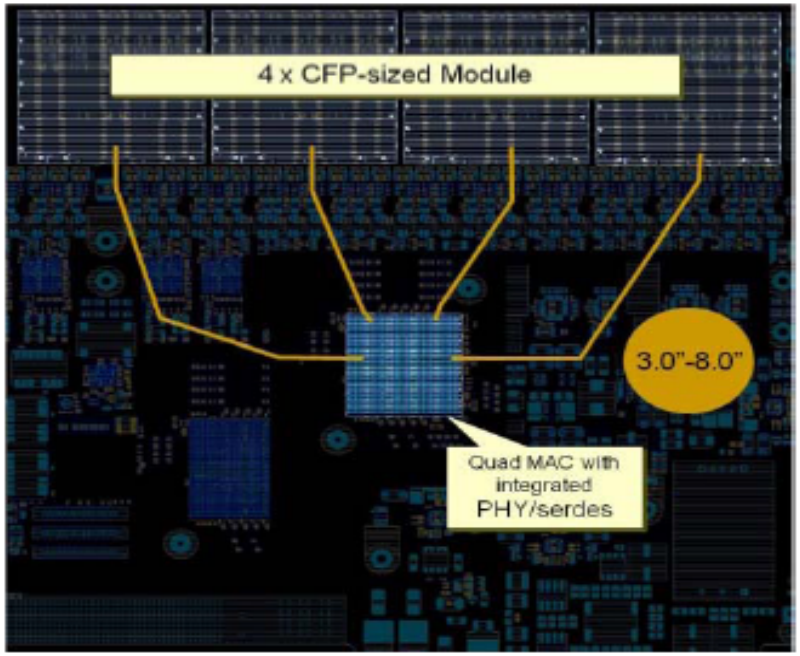
Unretime Applications Diagram with QSFP28

- Follows SFP+/QSFP+ model of lower power and cost trend
  - 802.3bj is defining CR4 to support 100GBase-CR4
  - It is unlikely 100GNGOPTX will define cPPI-4 due to complexity and current focus of the group on the optical PMDs

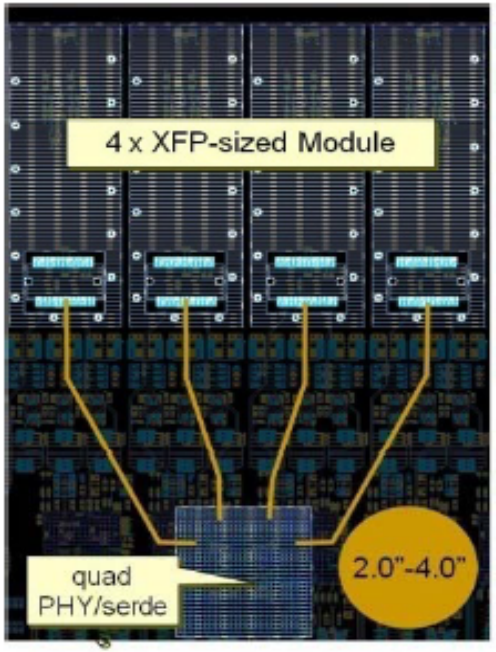


The Crystal Ball is not so clear!

- Nicholl_01_1111 assumes 1st generation 100 GbE implementation where gearbox chip placed 100 mm from the module
  - 2nd and 3rd generation 100GbE implementations single ASIC will connect to 16-32 ports
  - Linecard chip to chip applications require 300 mm PCB plus one connector



4 port CFP



4 port 'XFP'

PCB Reach for Various Interfaces

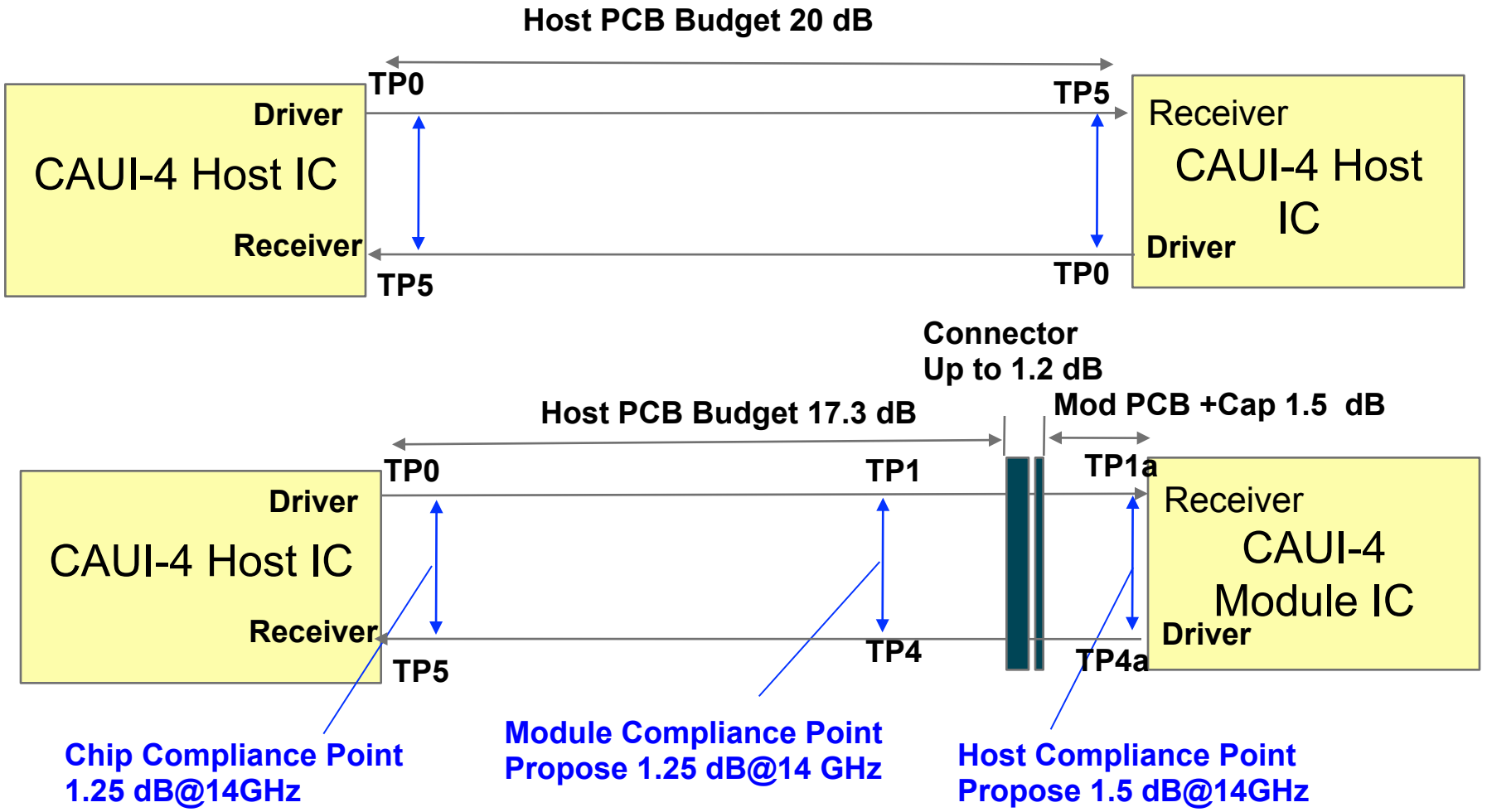
- PCB loss estimate assumptions and tools for calculation
  - IEEE 803.bj spreadsheet http://www.ieee802.org/3/bj/public/tools/DkDf_AlgebraicModel_v2.02a.xlsm for N4000-13SI and Megtron-6 calculation
  - Rogers Corp impedance calculator (free download but require registration) https://www.rogerscorp.com/acm/technology/index.aspx for FR4-6 and N4000-13
  - Stripline ~ 50 Ω, trace width is 5 mils, and with ½ oz Cu
  - Surface roughness med per IEEE spreadsheet or 2.8 um RMS
  - FR4-6 DK=4.2 and DF=0.02, N4000-13 DK=3.6 and DF=0.014, N4000-13SI and Meg-6 per IEEE spreadsheet

Host Trace Length (in)	Total Loss (dB)	Host Loss(dB)	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal PCB Loss/in at 5.15 GHz	N/A	N/A	1.00	0.79	0.56	0.43
Nominal PCB Loss/in at 12.89 GHz	N/A	N/A	2.00	1.60	1.25	0.92
CAUI Classic	10.5	7.9	7.9	10.0	14.1	18.4
PPI CL85A/86A with one connector & HCB#	6.5	4.37	4.4	5.5	7.8	10.2
OIF 28G-VSR with one connector & HCB*	10	6.8	3.4	4.3	5.4	7.4
802.3bj CL92A with one connector & HCB **	10	6.31	3.2	3.9	5.0	6.9
OIF 28G-SR with one connector & HCB*	15.4	12.2	6.1	7.6	9.8	13.3
OIF 28G-MR with one connector & HCB*	20	16.8	8.4	10.5	13.4	18.3

Assumes connector loss is 0.87 dB, HCB loss is 1.26 dB, 0 dB allocated for via loss.
* Assumes connector loss is 1.2 dB, HCB loss is 1.5 dB, 0.5 dB allocated for via at 12.89 GHz.
** Assumes connector loss is 1.69 dB, HCB loss is 1.5 dB, 0.5 dB allocated for via at 12.89 GHz.

Proposed CAUI-4 Architecture and Reference Points

- Following 802.3 CL83A/B (CAUI) where common I/O supports chip to chip and chip to module



CAUI-4 Having 20 dB (MR) vs 10 dB (VSR) Loss Budget

- Transmitter architecture
  - 3 tap FFE with pre and post for both MR/VSR
- Transmit amplitude
  - VSR is 600 mV
  - MR is 800 mV
- Receiver architecture
  - VSR assumes adaptive CTLE with 0-8 dB peaking
  - MR would require CTLE + about 2 tap DFE
- Receiver sensitivity
  - VSR at chip ball is 100 mV when measured with software CTLE
  - MR at chip ball likely 100 mV but with CTLE+2DFE
- Back channel
  - VSR has no back channel and is a symmetrical interface
  - MR may require back channel and is a symmetrical interface
- Power dissipation of adding 2 tap DFE is less than 1 CMOS node.

Summary

- Next generation 100 GbE line cards and module require a harmonious retime interface comparable to 10G CAUI
  - Support chip to chip applications with one connector & 250 mm of PCB
  - Support chip to module applications with one connector & 250 mm of PCB
- OIF 28G-VSR is an interim solution for retime chip to module
  - Designed around 1st generation implementation with gearbox chip placed very close to the module therefore the 100 mm PCB reach is sufficient
  - Next generation Switch/ASIC with integrated 25G I/O require 250 mm of PCB reach, if one uses VSR it will require mid-span retimer
  - OIF VSR doesn't meet next generation chip to chip or chip to chip line card applications but severing very important market need right now
- 100GNGOPTX likely will not defining unretime cPPI-4 due to complexity of the interface and current group focus on optical PMDs
  - Longer term unretime cPPI-4 offers more flexible architecture with lower cost and power as we have seen with SFP+/QSFP+
- 802.3bj currently defining unretime CR4
  - Host PCB reach vs cable reach should be optimized based on cable-host trade off and commonality with retime interface should not be a factor.

Thank You