DVCon India 2024: Selected Posters List

P1:315 - Design and Implementation of a Protocol-Agnostic Serial Bus Analyzer for Real-Time Waveform Debugging and Verification *Harshal Advane, Marvell*
P2:1079 - Leveraging AI/ML Models for Enhanced VLSI Design and Verification *Ayush Jain and Sudha Jain, onsemi*
P3:1946 - Framework for Automated Connectivity Checks for core and SOCs *Avinaba Tapadar, Akash Singh, Mohit Solanki, Raghu B R and Srobona Mitra, Qualcomm*
P4:2432 - Methodology for SDF back annotated Gatesims for a Mixed signal IP *Saksham Soni, Nilay Desai and Amlan Chakrabarti, AMD*
P5:3022 - A New Approach Of Hardware Verification Through Natural Language Queries *Priya Aggarwal, Samuel Katapur, Parth Bhatia, Viral Sharma and Nusrat Ali, TI*
P6:3800 - Enhanced SoC DV Infrastructure for expediting multi-chiplet boot using Ndie Simulation *Vignesh Adiththan, Vinay Swargam, Ayush Agrawal, Harshal Kothari and Madhukar Ramegowda, Samsung*
P7:3826 - An Efficient & Effective way Power Integrity Signoff for Long RTL Vectors *Abhinav Gaur, Akhilesh Mishra, Love Gupta and Manmeet Singh, NXP*
P8:4050 - Methodology for Efficient Fault Injection using Random Sampling *Vedant Garg, Prashantkumar Sonavane and James Kim, Synopsys, Samsung*
P9:4121 - Optimised Technique for Implementation of IOL Test-Suite *Vatsal Jain, Krishna Raman Singh and Anmol Kathuria, Siemens*
P10:4134 - Dynamically Configurable Generic Smart Interrupt Service Routine (ISR) Framework for Multi-Cluster 2.5D, 3DIC Chiplets *Padma Vutukuru, Lalithraj Mailappa and Sekhar Dangudubiyyam, Samsung*
P11:5391 - Digital Mixed Signal Verification Methodology for Highly Integrated Automotive RADAR SoC *Sainath Karlapalem, Atish Savale and Dheeraj B, NXP*
P12:6284 - Generic Configurable Checker Architecture for functional verification accelerated with AI/ML *Chandana Nallangi and Pavitra Balasubramanian, NXP.*
P13:6375 - Unleashing UCIe verification by capturing complex AI dataloads using distributed and ndie simulations for multi-chiplet SoC *Harshal Kothari, Vinay Swargam, Jerin M Jose, Jasobanta Sahoo and Madhukar Ramegowda, SSIR*

P14: 7039 - Automation of Glitch Checker Implementation on Various Design Interfaces/Boundaries *Nikhila Pranavi Adari, NXP*
P15: 7132 - Synergizing Functional Safety and Fault Simulation: Towards Robust and Reliable Systems in Safety-Critical SoCs *Santosh Mahale and Shantanu Lele, Marvell*
P16: 5342 - ML based regression accelerator *Nikhil Singla, Pandithurai Sangaiyah and Rohit Jindal, GOOGLE*
P17: 7968 - GEN AI based assertion code pattern generation *Mrinal Kar, Yash Kumar, Rohit Kumar, Karthikeyan Sundaram, Sathish Kumar K, Manikandan S, Murthy Siriginedi Nvs and Sharan Basappa, HCL*