ROHM Solution Simulator
Power Device Use's Guide
for PFC Circuits

User's Guide

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Introduction

This user's guide summarizes the basic adjustment methods and know-how of each parameter so that users can fully utilize the PFC circuit of the "Power Device Solution circuit". We introduce specific solutions for each theme that is likely to be a bottleneck in designing a PFC circuit. Please use it as a reference when facing a trouble like "the circuit does not work well" or "need to optimize the circuit conditions more".
In addition, "inverter edition" and "DC-DC converter edition" will be released later, so please use them as well.

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1. PFC circuit list

Table 1 shows the PFC circuits registered in "Power Device Solution circuit". Reference circuits cover commonly used 4 categories such as “Boundary Current Mode (BCM)”, ”Continuous Current Mode (CCM)”, “Discontinuous Current Mode (DCM)” and high-power “3-phase PFC”. In addition to the basic “single boost PFC” various reference circuits are prepared such as ”Interleaved PFC”, “synchronous rectification”, “bridgeless”, and “Totem-pole”, so please use them according to your needs.

Class	ID Number	Circuit name
PFC Boundary Current Mode (BCM)	A-1	PFC BCM Vin=200V Iin=2.5A
	A-2	PFC BCM Diode-Bridge-Less Vin=200V Iin=2.5A
	A-3	PFC BCM Diode-Bridge-Less Vin=200V Iin=50A
PFC Continuous Current Mode (CCM)	A-4	PFC CCM Vin=200V Iin=2.5A
	A-5	PFC CCM 2-Phase Vin=200V Iin=5A
	A-6	PFC CCM Synchro Vin=200V Iin=2.5A
	A-7	PFC CCM Synchro 2-Phase Vin=200V Iin=5A
	A-8	PFC CCM Diode-Bridge-Less Synchro Vin=200V Iin=50A
	A-9	PFC CCM Diode-Bridge-Less Full-Bridge Vin=200V Iin=20A
	A-10	PFC CCM Totem-Pole Synchro Vin=200V Iin=100A
PFC Discontinuous Current Mode (DCM)	A-11	PFC DCM Vin=200V Iin=2.5A
	A-12	PFC DCM 2-Phase Vin=200V Iin=5A
	A-13	PFC DCM 3-Phase Vin=200V Iin=7.5A
	A-14	PFC DCM Synchro Vin=200V Iin=2.5A
	A-15	PFC DCM Synchro 2-Phase Vin=200V Iin=5A
	A-16	PFC DCM Synchro 3-Phase Vin=200V Iin=7.5A
	A-17	PFC DCM Diode-Bridge-Less Synchro Vin=200V Iin=50A
PFC 3-Phase	A-18	PFC 3-Phase 3-Wire Vin=200V Pin=25kW
	A-19	PFC 3-Phase 4-Wire Vin=115/200V Pin=25kW

Table 1. List of PFC circuits in Power Device Solution Circuit

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2. Adjustment of Inductance L

This chapter will show you how to adjust the inductance L to get the proper ripple rate of inductor current. The operation mode here is premised on CCM (Continuous Current Mode).

2-1. Circuit example

Figure 1 "A-4 PFC CCM Vin = 200V Iin = 2.5A" will be explained as an example. The conditions in the yellow box will be changed and then L value will be adjusted based on the changed conditions.

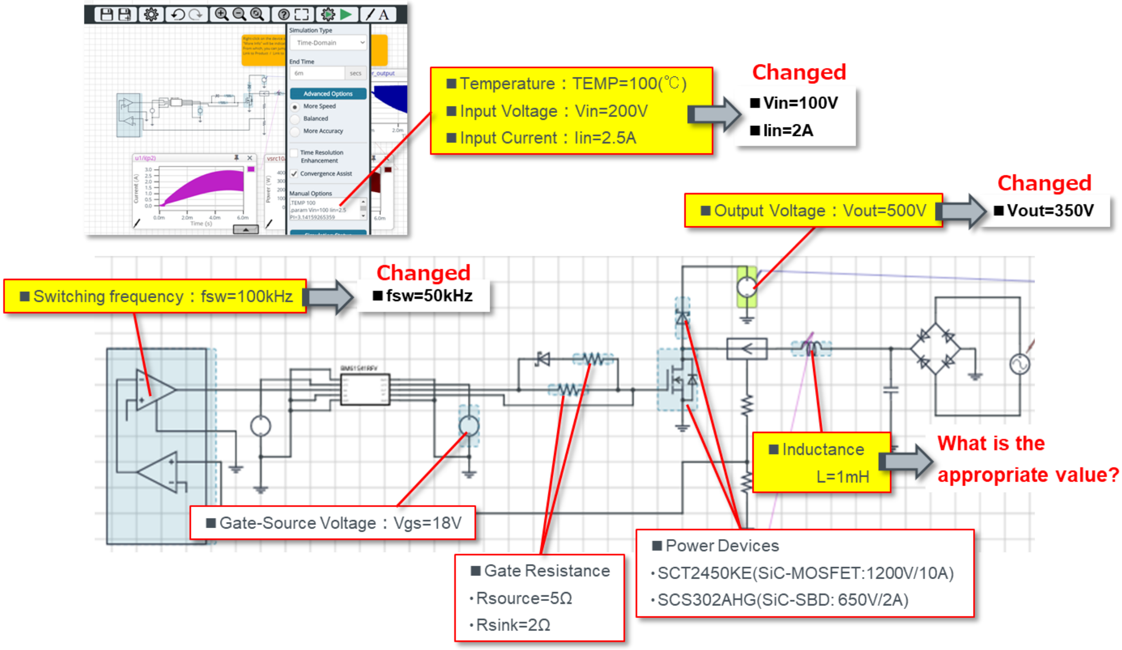

Figure 1. Circuit example "A-4 PFC CCM Vin=200V Iin=2.5A"

2-2. Ripple rate M before adjusting the inductance L

Figure 2 shows the inductor current I_L before adjusting the inductance L (default value: 1mH).
The peak value of I_L is $I_{L\_peak} \approx 3.7A$.

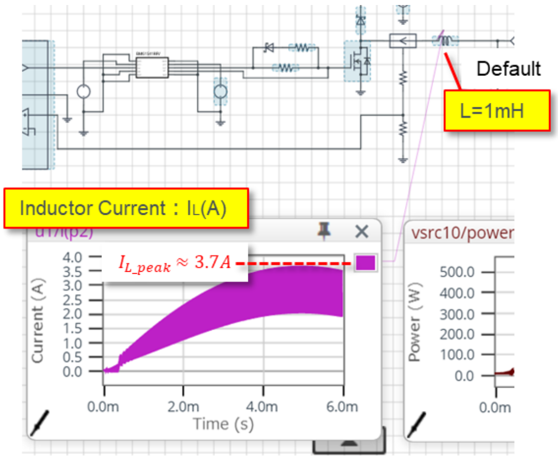

Figure 2. Inductor current before adjusting inductance L

Also, since the peak value of the input current is $I_{in\_peak} = \sqrt{2} \times I_{in} \approx 2.82A$, the ripple rate M is calculated as

$$\text{Ripple rate } M = \left(I_{L\_peak} - I_{in\_peak}\right) / I_{in\_peak} = (3.7 - 2.82) / 2.82 \approx 31.2\%$$

Since the ripple rate is generally set to less than 30%, it is necessary to adjust inductance value to reduce the ripple rate.

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2-3. How to adjust the inductance L

Inductance L can generally be described by the following.

$$L = \{(V_{out} - \sqrt{2} \times V_{in}) \times \eta \times {V_{in}}^2\}/(f_{sw} \times M \times P_{out} \times V_{out})$$

η: Efficiency, M: Ripple rate

Estimation of an appropriate value of L with η=0.95 and M=0.3 is as follows.

$$L = \{(350 - \sqrt{2} \times 100) \times 0.95 \times 100^2\}/(50{,}000 \times 0.3 \times 200 \times 350) \approx 1.89[mH]$$

From the above estimation, re-simulation is performed with a new inductance of 2mH. The peak value of inductor current is $I_{L\_peak} \approx 3.4A$ as shown in Figure 3.

Therefore, the ripple rate is $M = (3.4 - 2.82) / 2.82 \approx 20.6\%$, which is successfully adjusted to less than 30%.

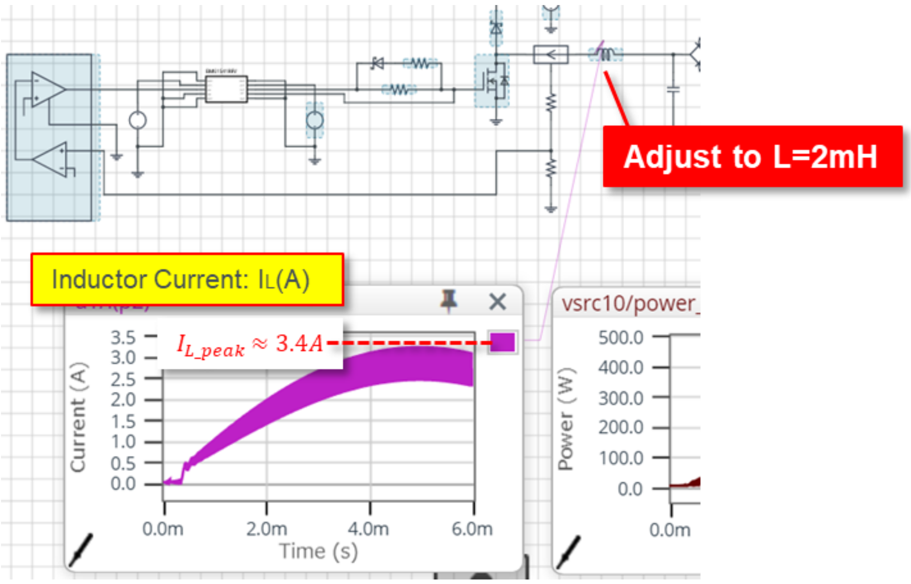


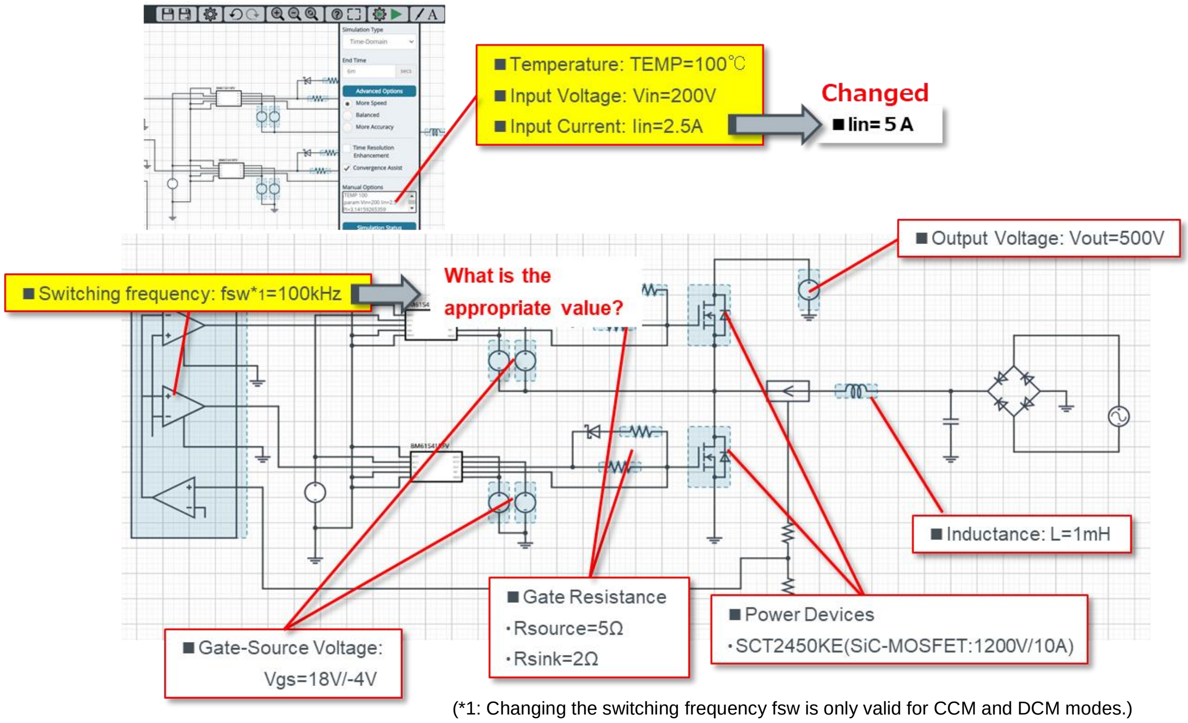
Figure 3. Inductor current after adjusting the value of L

3. Adjustment of switching frequency fsw

This chapter will show you how to adjust the switching frequency fsw to get the appropriate value for the inductor current ripple rate. The operation mode here is premised on CCM (Continuous Current Mode).

3-1. Circuit example

Figure 4 " A-6. PFC CCM Synchro Vin=200V Iin=2.5A " will be explained as an example. The conditions in the yellow box will be changed and then fsw value will be adjusted based on the changed conditions.



(*1: Changing the switching frequency fsw is only valid for CCM and DCM modes.)

Figure 4. Circuit example "A-6. PFC CCM Synchro Vin=200V Iin=2.5A"

3-2. Ripple rate before adjusting switching frequency fsw

Figure 5 shows the inductor current I_L before adjustment of switching frequency fsw (default value: 100kHz). The peak value of I_L is $I_{L\_peak} \approx 7.8A$.

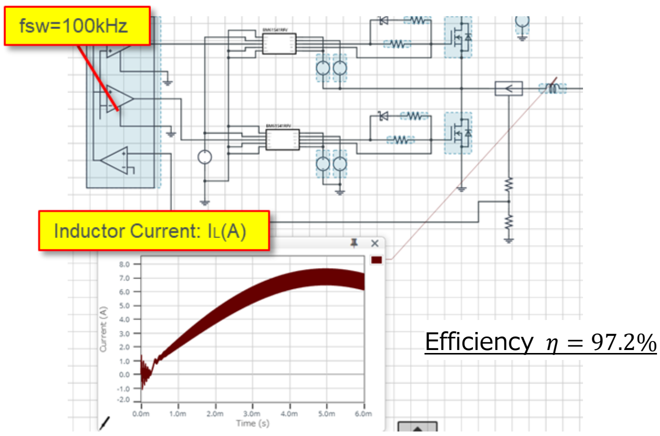


Figure 5. Inductor current before adjusting switching frequency fsw

The peak value of the input current is $I_{in\_peak} = \sqrt{2} \times I_{in} \approx 7.07A$, so the ripple rate M is calculated as follows.

$$\text{Ripple rate } M = (I_{L\_peak} - I_{in\_peak}) \,/\, I_{in\_peak} = (7.8 - 7.07) \,/\, 7.07 \approx 10.3\%$$

This ripple rate is small enough, so consider reducing fsw to improve efficiency. The efficiency before adjusting fsw is η =97.2%.

3-3. How to adjust the switching frequency fsw

The switching frequency fsw can generally be described by the following.

$$fsw = \{(V_{out} - \sqrt{2} \times V_{in}) \times \eta \times V_{in}{}^{2}\} \,/\, (L \times M \times P_{out} \times V_{out})$$

η: Efficiency, M: Ripple rate

Estimation of an appropriate value of fsw with η=0.972 and M=0.3 is as follows.

$$fsw = \{(500 - \sqrt{2} \times 200) \times 0.95 \times 200^2\}/(0.001 \times 0.3 \times 1000 \times 500) \approx 56.3\ [kHz]$$

From the above estimation, re-simulation is performed with a new fsw of 55kHz. The peak value of inductor current is $I_{L\_peak} \approx 8.5A$ as shown in Figure 6.

Therefore, the ripple rate is $M = (8.5 - 7.07) \,/\, 7.07 \approx 20.2\%$, and the efficiency is η= 97.3%, which is 0.1% higher than before fsw adjustment.

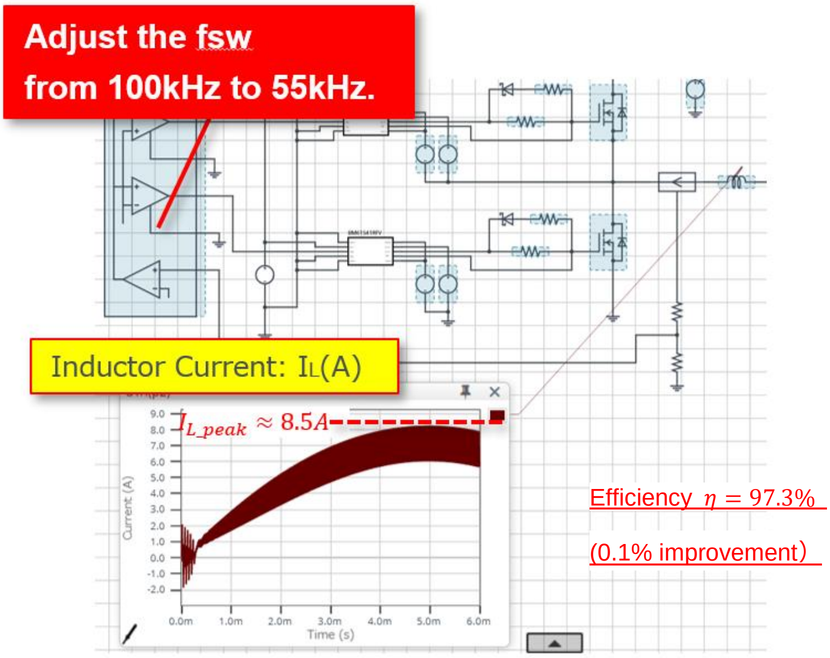


Figure 6. Inductor current after adjusting switching frequency fsw

4. Consideration of appropriate value of gate-drive voltage Vgs

In this chapter, we will consider the appropriate value of gate-drive voltage Vgs, especially for SiC MOSFETs.

4-1. Circuit example

Figure 7 "A-2. PFC BCM Diode-Bridge-Less Vin=200V iin=2.5A" will be explained as an example.
Consider the appropriate Vgs value to drive the low-side switching device "SCT2450KE (SiC MOSFET)".

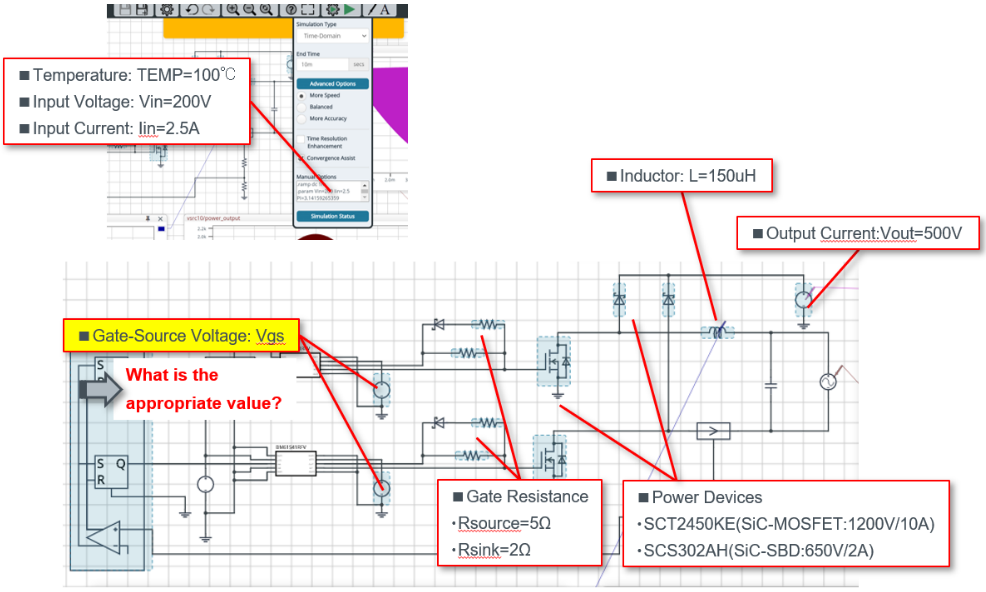


Figure 7. Circuit example "A-2. PFC BCM Diode-Bridge-Less Vin=200V Iin=2.5A"

4-2. Correlation between on-resistance Ron and gate-drive voltage Vgs

As shown in Figure 8, on-resistance Ron of the conventional Si-MOSFETs is almost constant even if Vgs changes in the on state. On the other hand, in SiC MOSFETs, Ron changes greatly according to the change of Vgs value as shown in Figure 9. Therefore, setting the Vgs value is more important than Si-MOSFETs.

In other words, in SiC MOSFETs, if Vgs value is low, conduction loss increases and efficiency decreases. On the contrary, if Vgs value is raised too much in order to improve efficiency, the rating will be exceeded. For these reasons, properly configuring Vgs value is very important.

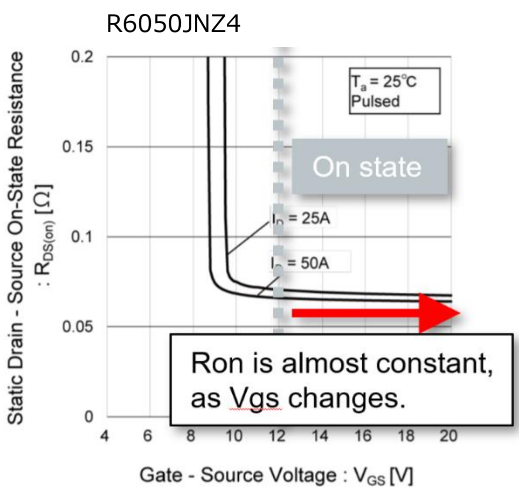


Figure 8. Ron vs. Vgs in Si-MOSFET

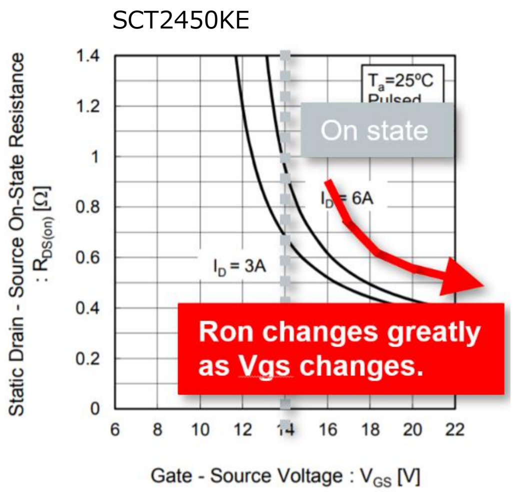


Figure 9. Ron vs. Vgs in SiC MOSFET

4-3. Consideration of appropriate value of gate-drive voltage Vgs

Figure 10. shows the efficiency simulation results when the Vgs value is changed in the circuit "A-2 PFC BCM Diode-Bridge-Less Vin = 200V Iin = 2.5A" in the previous section 4-1.

When Vgs value is 14V or less, the efficiency drops sharply due to the increase in on-resistance Ron. This tendency becomes more pronounced at lower temperatures. Usage in this Vgs range is prohibited because the risk of device destruction increases. On the contrary, the higher the Vgs, the better the efficiency, but please do not exceed the maximum rating (Vgs= 22V).

Therefore, considering the balance between efficiency and safety, it can be said that gate driving at around Vgs=18V*[1] is appropriate.

（*1: ROHM's SiC MOSFETs are generally recommended to be used at around Vgs=18V.）

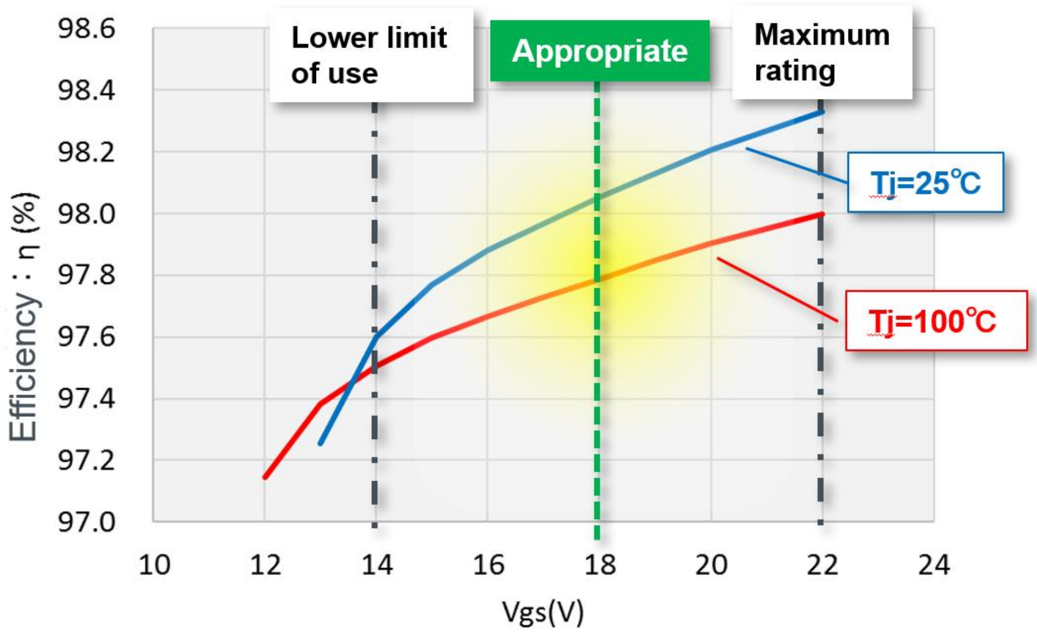


Figure 10. Simulation result "Efficiency vs. Vgs".

5. Optimization of gate resistance Rg

Noise reduction is a major issue in actual circuit design. Generally, increasing the gate resistance Rg can suppress noise, but on the contrary, it is inefficient (large loss), so it is very important to set the Rg value appropriately.
In this chapter, we will consider how much the gate resistance Rg can be increased for a noise reduction while keeping the loss of MOSFET to a certain value or less (assuming 5W or less).
Note that noise evaluation requires actual circuit evaluation, so it is omitted in this document.

5-1. Circuit example

Figure 11 "A-5. PFC CCM 2-Phase Vin=200V Iin=5A " will be explained as an example.
We will consider how much Rg can be increased while keeping loss of the low-side SiC MOSFET SCT2450KE to 5W or less*1.
(*1: This condition is just an example, so please modify it with usage condition.)

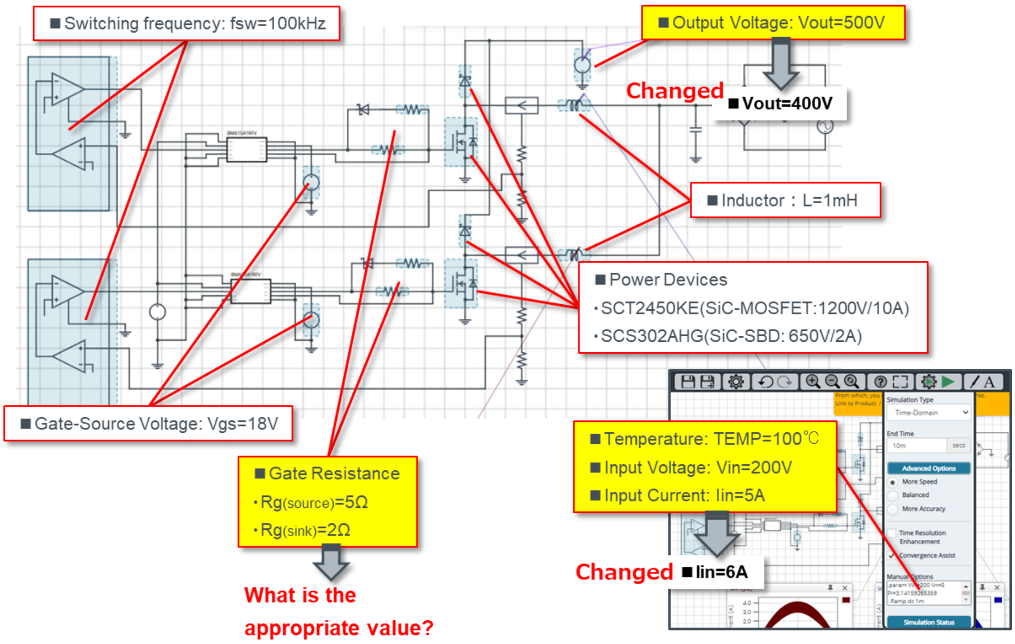


Figure 11. Circuit example "A-5. PFC CCM 2-Phase Vin=200V Iin=5A"

5-2. Correlation between Rg and switching loss

Figure 12 shows the correlation between switching loss, drain current I_D, drain-source voltage V_{DS}, and gate-source voltage Vgs at turn-on. These period t1 and t2 when switching loss occurs can be described as follows.

$$t1 = \boldsymbol{Rg} \times (Cgs + Cgd) \times \ln\left(\frac{Vgs - Vth}{Vgs - VGP}\right)$$

$$t2 = Qgd \times \boldsymbol{Rg} / (Vgs - VGP)$$

From these, the period t1 and t2 are proportional to Rg.
Since I_D and V_{DS} change almost linearly in these period, switching loss is almost proportional to Rg as well.

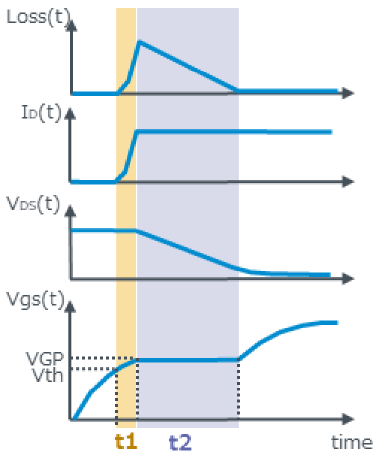


Figure 12.
Correlation between switching loss, I_D, V_{DS} and V_{gs} at turn-on

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5-3. Optimization of gate resistance Rg

Figure 13. shows the simulation results for MOSFET loss with different Rg. For the sake of clarity, the resistance values on the "source side" and "sink side" are changed with the same ratio.

The result shows conduction loss is constant because it is not affected by Rg, and switching loss is proportional to Rg as described in Section 5-2. In order to suppress the loss below 5W, the magnification ratio of Rg should be set to 9 times or less of the initial, that is, **Rg(source)<45Ω and Rg(sink)<18Ω**

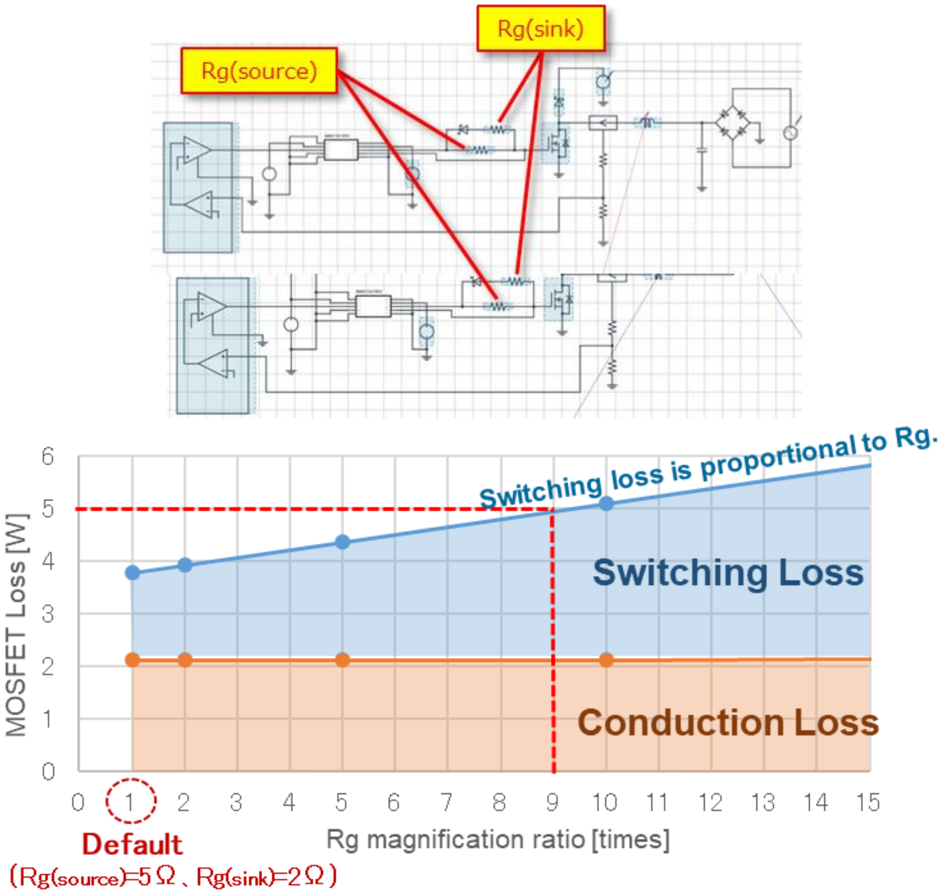

Figure 13. Simulation results for MOSFET loss vs. Rg

6. Optimum value of Dead Time

In this chapter, we will consider how to estimate the optimum (shortest possible without shoot-through current) value of Dead Time in a bridge circuit.

6-1. Circuit example

Figure 14 " A-6. PFC CCM Synchro Vin=200V Iin=2.5A " will be explained as an example.
Optimum value of Dead Time is considered for the synchronous rectification bridge topology using SiC MOSFET SCT2450KE. Dead Time can be set by the PWM controller TD1 (high side) and TD2 (low side), respectively.

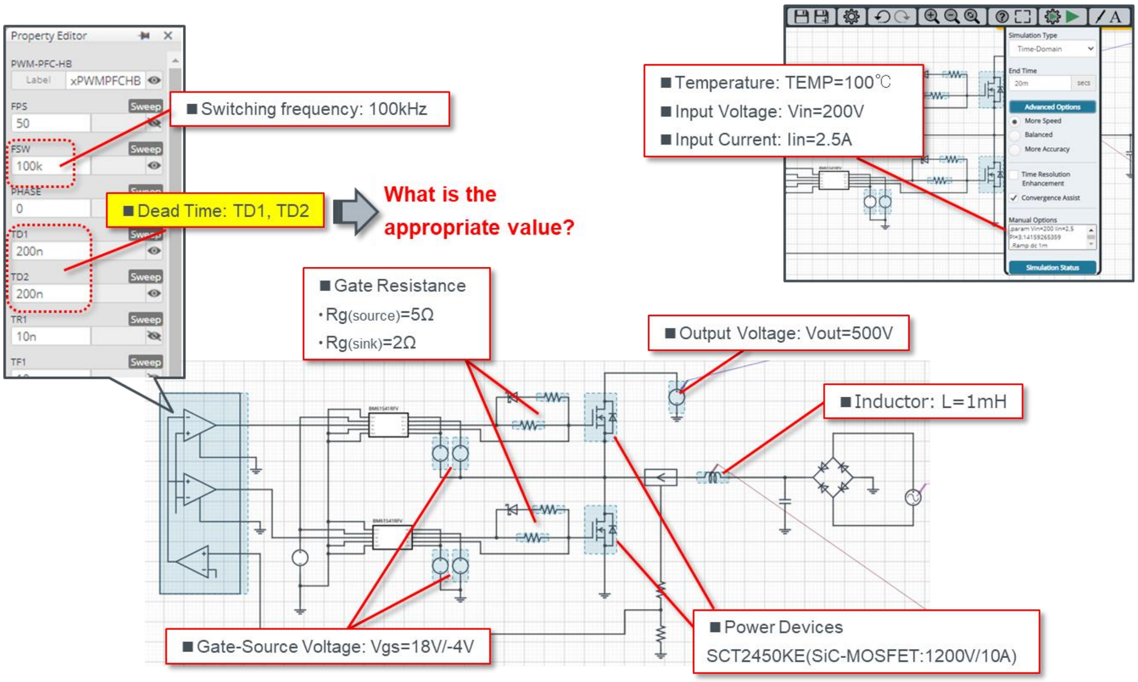

Figure 14. Circuit example "A-6. PFC CCM Synchro Vin=200V Iin=2.5A"

6-2. Loss in the Dead Time period

Figure 15 shows the current flow during the Dead Time period. "HS" means "high side" and "LS" means "low side".
In a bridge configuration, the Dead Time must be long enough to prevent shoot-through current from flowing. However, be aware that if you set the dead time unnecessarily long, the loss will increase. The reason for this is that during the Dead Time period, the channel of the MOSFET is OFF state and the current flows through the built-in diode with a large conduction loss.

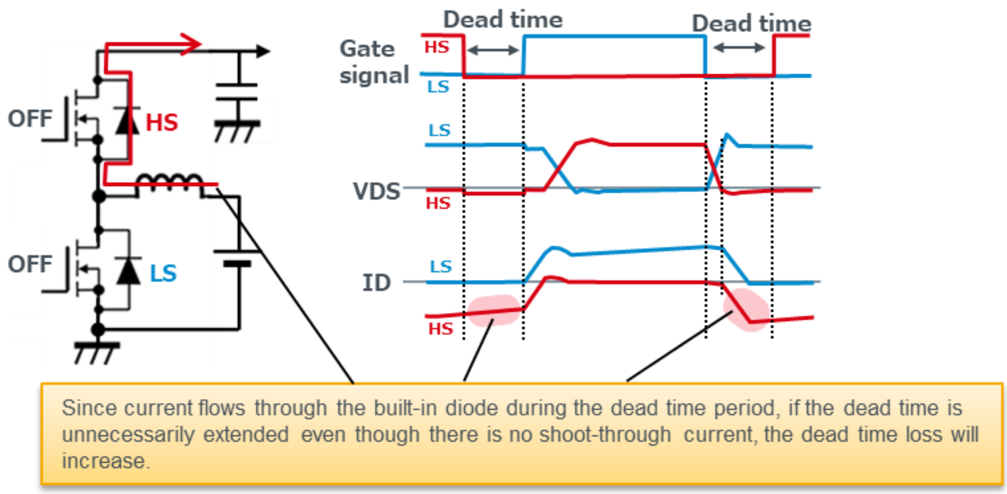

Figure 15. Current flow during the Dead Time period

6-3. Correlation between Dead Time and power factor

Figure 16. shows the correlation between the Dead Time length and the inductor current I_L in the PFC circuit. If the Dead Time is too long, discontinuous operation may occur when input AC voltage is low, resulting in distortion of the inductor current waveform and a decrease in power factor. Therefore, setting the Dead Time unnecessarily long is not preferable from the viewpoint of power factor.

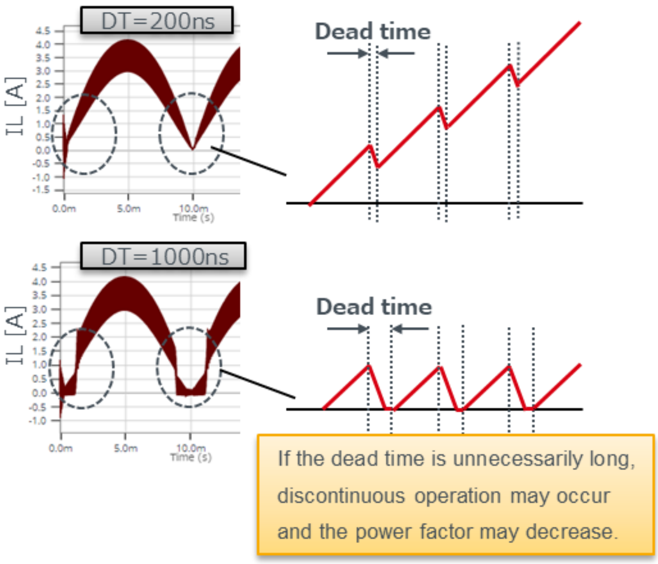

Figure 16. Correlation between Dead Time and Inductor Current I_L

6-4. Consideration of the optimum Dead Time length

Figure 17. shows the simulation results showing the correlation between MOSFET loss and Dead Time length. "HS" means "high side" and "LS" means "low side".

When the dead time is set to 50ns or less, the loss will increase sharply due to the shoot-through current. On the contrary, if the Dead time is extended, the conduction time of the HS-MOSFET built-in diode becomes longer, so the loss increases. The MOSFET loss is minimized at T_D of 100ns when Dead Time is the shortest without shoot-through current. However, since the switching speed depends on the temperature and lot-to-lot variation, it is generally necessary to keep a margin of about 100ns. Therefore, in this case, **Dead time of 200ns** is the best.

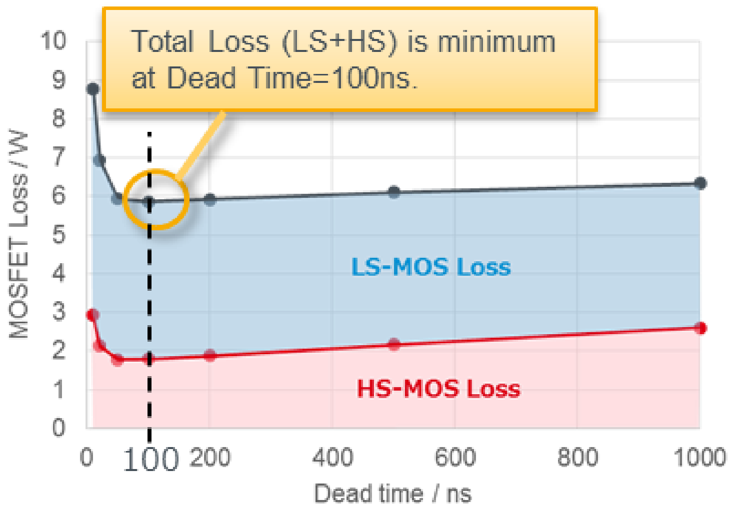

Figure 17. Correlation between MOSFET loss and Dead Time length (simulation)

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