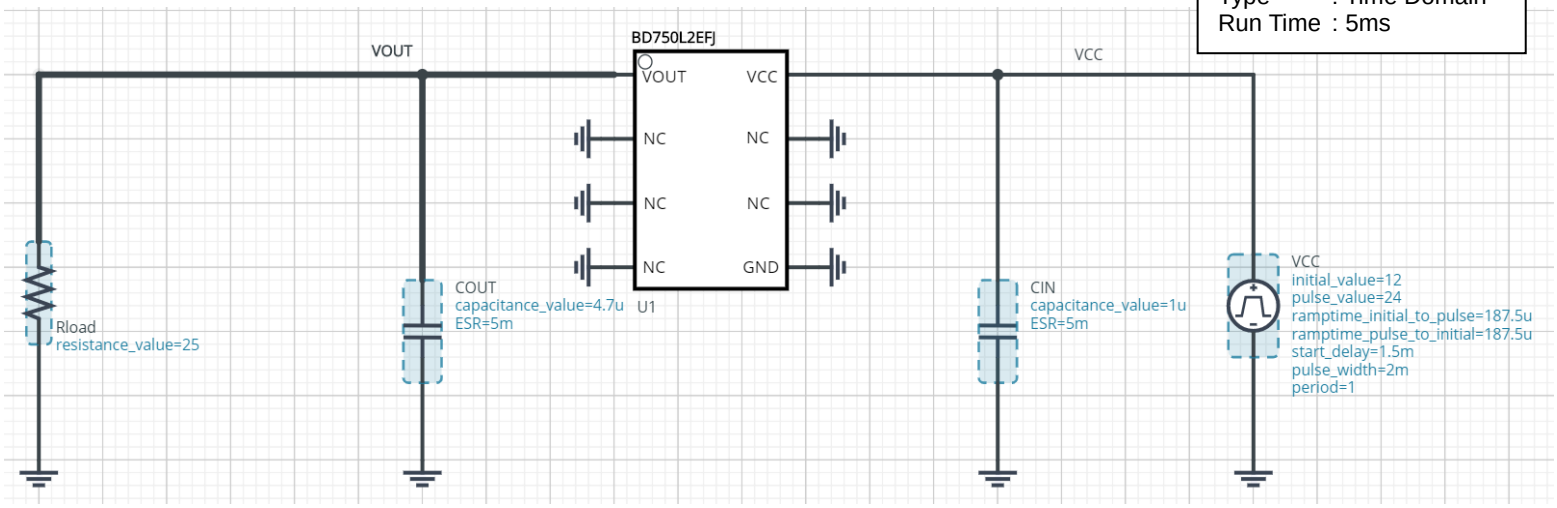
Ultra Low Quiescent Current LDO Regulator

BD750L2EFJ / Line Response

This Circuit simulates the Line Response.
You can check the fluctuation of the output voltage when the input voltage is abruptly changed.

Simulation Schematic

Simulation Setting
Type : Time Domain
Run Time : 5ms



Peripheral Components

Instance Name	Type	Parameter	Default Value	Variable Range		Unit
				Min	Max	
CIN	Capacitor	capacitance_value	1	0.1	no constraint(Note 1)	µF
		ESR	5	1	10000	mΩ
COUT	Capacitor	capacitance_value	4.7	4.7	no constraint(Note 1)	µF
		ESR	5	1	10000	mΩ

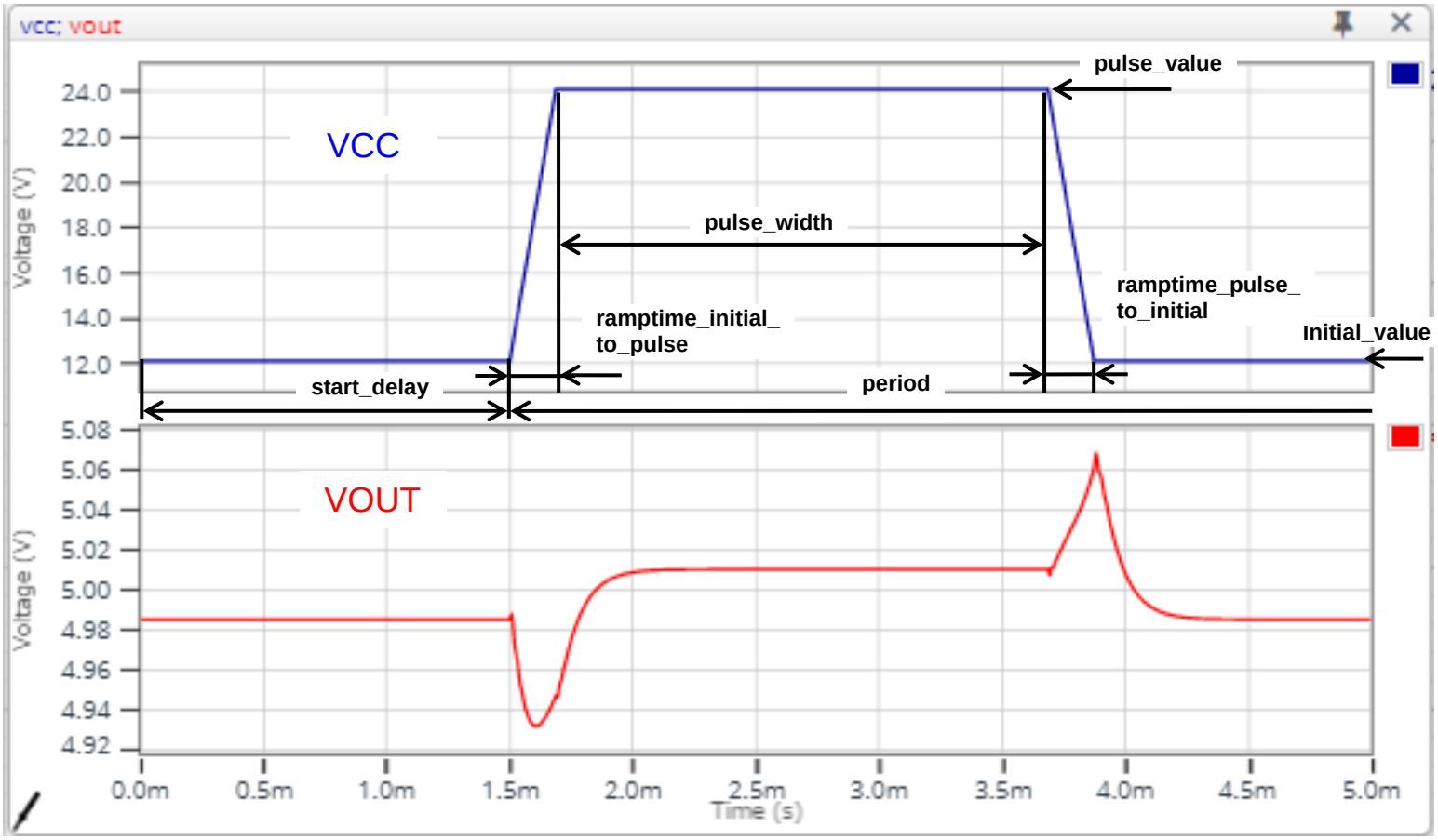
Simulation Conditions

Instance Name	Type	Parameter	Default Value	Variable Range		Unit
				Min	Max	
VCC	Voltage Source	initial_value	12	5.8	45	V
		pulse_value	24	5.8	45	V
		ramptime_initial_to_pulse	187.5	no constraint(Note 1)		µs
		ramptime_pulse_to_initial	187.5	no constraint(Note 1)		µs
		start_delay	1.5	no constraint(Note 1)		ms
		pulse_width	2	no constraint(Note 1)		ms
		period	1	no constraint(Note 1)		s
Rload	Resistor	resistance_value	50	25	100M	Ω

(Note 1) This is a constraint of the simulation settings and does not guarantee the operation of the IC.

Caution 1: The values from the simulation results are not guaranteed. Please use these results as a guide for your design.
Caution 2: These model characteristics are specifically at Ta=25°C. Thus, the simulation result with temperature variances may significantly differ from the result with the one done at actual application board (actual measurement).
Caution 3: Please refer to the datasheet for details of the technical information

Simulation Result



Notes

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3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
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