Double Pulse Test Simulation with P05SCT4018KR-EVK-001 Simulation Model

2022. Feb
64UG137E Rev.001

<Getting Started>

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How to use ROHM Solution Simulator

Please visit ROHM Solution Simulator page
(https://www.rohm.com/solution-simulator)

- Hands-On User's Manual Link
- Tutorial Short Videos available

P05SCT4018KR-EVK-001_DPT_HS

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<Outlines>

This double pulse test simulation circuit is based on the circuit configuration of ROHM’s "4th Generation SiC MOSFET Half Bridge Evaluation Board" P05SCT4018KR-EVK-001 and reflects the parasitic components of the PCB wiring pattern based on electromagnetic field analysis. By modeling the EVK implementation and reflecting it in the simulation, it is now possible to accurately simulate the switching waveforms of the actual device.

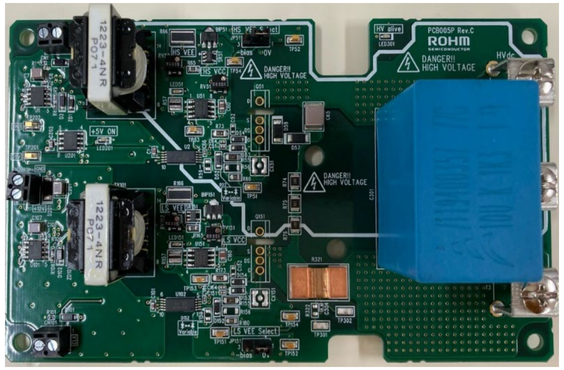

Figure 1. P05SCT4018KR-EVK-001

Features

- Double pulse test circuit (High-side switching)
- 4th generation SiC MOSFET SCT4018KR + gate driver IC BM61S41RFV-C.
- Device equivalent circuit model of the components are used for simulation accuracy.
- Parasitic inductors of PCB patterns are modelled and applied to the simulation circuit.
- Vgs, VDC, snubber circuit constants, etc. can be modified.
- Approx. simulation elapsed time is 2min30s.

Applications

- By simulating and verifying the operating conditions and circuit constants of drive circuits, etc., the workload of hardware evaluation can be reduced.
- By extracting the parasitic L of the pattern from the PCB layout and adding it to the circuit for simulation, it is possible to improve the problem before prototyping.
- Simulation with the EVK detailed model may help to analyze the cause of noise surge surges observed in the hardware evaluation.

Note) For more details of P05SCT4018KR-EVK-001, please refer to the following documents.
4th Generation SiC MOSFET Evaluation Board Product Specifications.pdf
4th Generation SiC MOSFET Evaluation Board User’s Manual.pdf

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<Simulation Circuit>

Table 1. Parameter Settings

Parameters	Descriptions	Default	Simulation Setting Range
VDC	DC Voltage	800 V	
HS_VCC2, LS_VCC2	Gate drive positive voltage	18 V	15 to 20 V
HS_VEE, LS_VEE	Gate drive negative voltage	0 V	0 to 4 V
Tj	Q51, Q151 Device Junction Temperature	25 °C	
HS_VPULSE	High-side pulse period	5 μs	Fixed
	Low-side pulse width	2.4 μs	
LS_VPULSE	"L" (DC)		

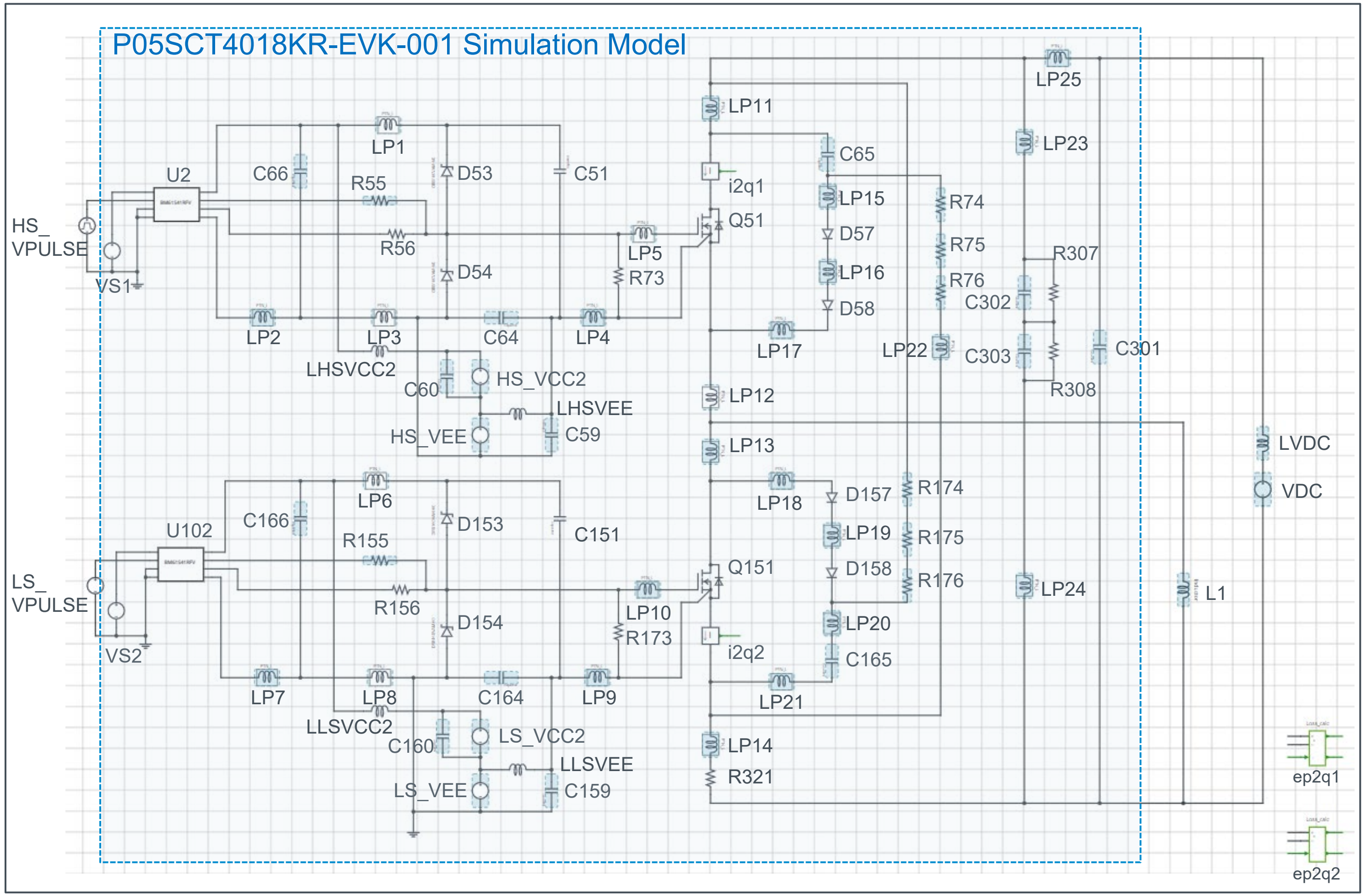

Figure 2. Simulation Circuit

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<Simulation Settings>

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How to setup the gate drive pulse

1. **Gate drive voltage Vgs**

Figure 3 shows a simplified gate driver circuit, and Figure 4 shows an example of the Vgs waveform. The voltage source VEE gives the voltage of the DS pin of the SiC MOSFET with respect to the GND2 voltage of the gate driver IC. The voltage source VCC2 gives the supply voltage VCC of the gate driver IC with respect to the DS pin voltage. As a result, the gate voltage Vgs of the SiC MOSFET is VCC for 'H' voltage and (-VEE) for 'L' voltage.

Set HS_VCC and HS_VEE for the high-side circuit, and LS_VCC and LS_VEE for the low-side circuit, respectively.

2. **Gate Drive Pulse timing**

Voltage source 'HS_VPULSE' generate the gate drive pulse timing. The period T = 5µs and the pulse width = 2.5µs. The actual gate drive pulse output is at the 'out' pin of BM61S41RFV-C, the gate driver IC.

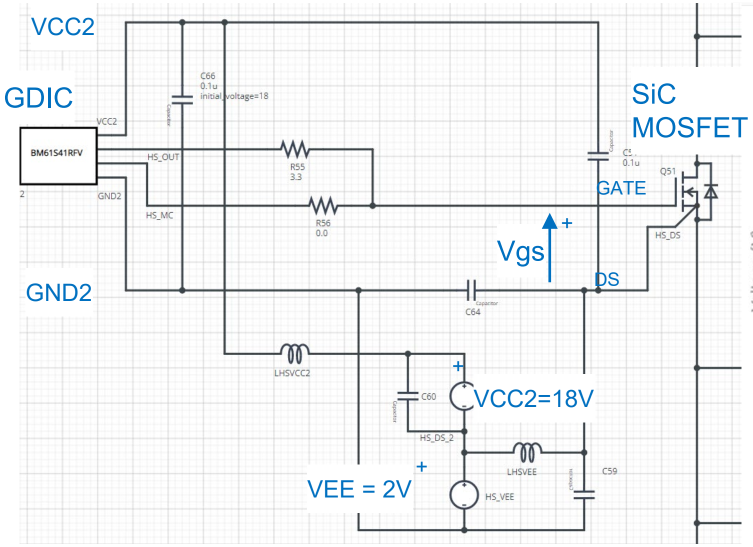

Figure 3. Simplified Gate Drive Circuit
(common for high-side and low-side)

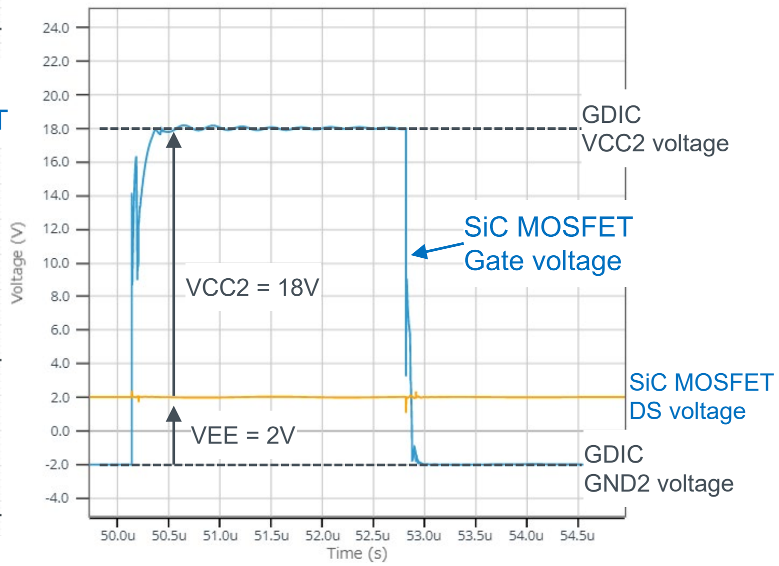

Figure 4. SiC MOSFET Vgs Voltage

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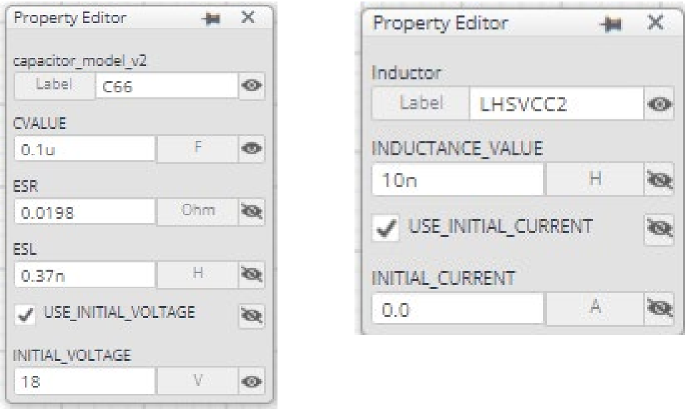
<Simulation Settings>

How to set simulation parameters

1. Using Property Editor

To open the Property Editor, right-click on a component and select "Properties" from the pull-down menu. Figure 5 shows an example of the Property Editor. You can browse the parameters of the component from the Property Editor.

Components shown in blue have “tunable" parameters, and you can change the parameters in the white text box in the Property Editor. Apply the values within the displayed tolerance range.



(a) Capacitor (b) Inductor

Figure 5. Property Editor Examples

2. ‘USE_INITIAL_VOLTAGE’ and ‘USE_INITIAL_CURRENT’

The capacitor property 'USE_INITIAL_VOLTAGE' and the inductor property 'USE_INITIAL_CURRENT' are used to improve the convergence of the simulation and speed up the simulation. Initial voltage or initial current value will be applied to the component as the initial condition. It will improve simulation convergence.
When changing simulation parameters, the initial voltage and the initial current should be revised.
Table 2 and Table 3 shows the recommendation of the initial voltage and the initial current.

Table 2. Initial Voltage Recommendation

Symbol	Initial Voltage Recommendation
C64, C164	(-HS_VEE), (-LS_VEE)
C66, C166	(HS_VEE+HS_VCC2), (LS_VEE+LS_VCC2)
C59, C159	HS_VEE, LS_VEE
C65, C165	VDC
C302, C303	(VDC/2)
C301	VDC

Table 3. Initial Current Recommendation

Symbol	Initial Current Recommendation
LP16	0
LP19	0
LP20	0

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<Component List>

Table 4. Power Device / Gate Driver IC Component List

Symbol	Part Number	Device
Q51, Q151	SCT4018KR	4G-SiC MOSFET, 1200V, 18mohm
D53, D54, D153, D154	RB160VAM-60	Schottky Barrier Diode
D57, D58, D157, D158	RFN1LAM7S	Super Fast Recovery Diode
U2, U102	BM61S41RFV-C	1ch Gate Driver Providing Galvanic Isolation

Part Number of Q51 and Q151 are selectable from the property editor.
The list of the part number is shown below.
To change the MOSFET, see instruction ‘How to change MOSFET model’ or refer to the hands-on manual from the link on Page 1.

Table 5. SiC MOSFET Part Number List

Symbol	Part Number	Features
Q51, Q151	SCT4018KR*	1200V, 18mohm
	SCT4036KR	1200V, 36mohm

* Default device

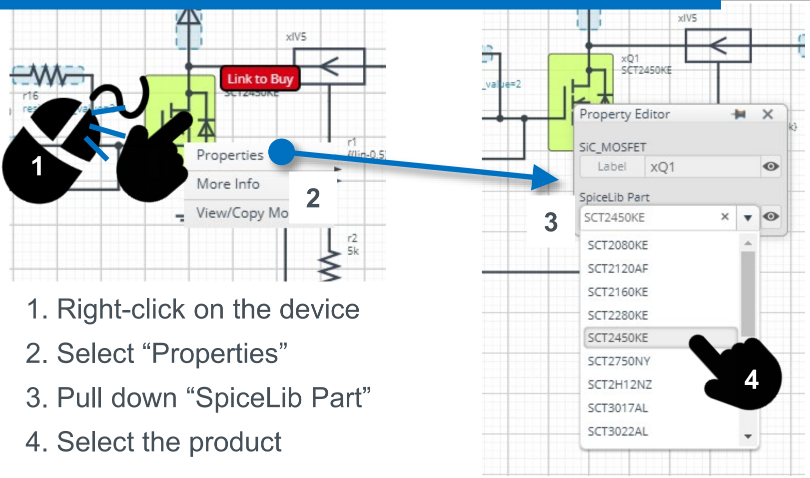
Note) We have not been able to confirm operation with all combinations.
Please read the disclaimer carefully.

Table 6. Resistor Component List

Symbol	R value [ohm]	Tun-able	Comments
R55, R155	3.3	✓	Gate resistors
R56, R156	0		
R73, R173	4.7k		
R74, R75, R76, R174, R175, R176	10	✓	RCD Snubber resistors
R307, R308	1M		C Snubber resistors
R321	0.1m		Shunt resistor

Note) The value is constant unless otherwise specified as ‘Tunable’.

How to change MOSFET Model



1. Right-click on the device
2. Select “Properties”
3. Pull down “SpiceLib Part”
4. Select the product

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<Component List>

Table 7. Inductor Component List

Symbol	Inductor Values					Simulation Settings	Descriptions
	L [H]	PAR_ RES [ohm]	SER_ RES [ohm]	PAR_ CAP[F]	Tun-able	Use Initial current = 0 Option	
L1	250μ	51k	0.13	2.124p	✓	✓	DPT Inductive Load

Note) Refer to Figure 5 for the model composition.
Note) The value is constant unless otherwise specified as ‘Tunable’.

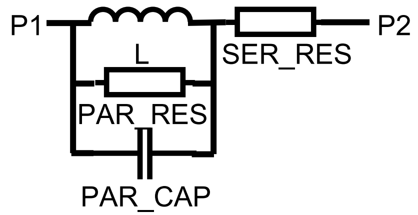

Figure 5. Inductor Model

Table 8. Capacitor Component List

Symbol	Capacitor Values				Simulation Settings			Descriptions
	C [F]	ESR [ohm]	ESL [H]	Tun-able	Initial Voltage [V]	Tun-able	Use Initial Voltage	
C51, C151	0.1μ	19.8m	0.37n		0			
C64, C164	0.1μ	19.8m	0.37n		0	✓	✓	
C66, C166	0.1μ	19.8m	0.37n		18	✓	✓	
C59, C159	4.7μ	3.2m	0.48n		0	✓	✓	
C60, C160	4.7μ	3.2m	0.48n		18	✓	✓	
C65, C165	33n	12m	0.65n	✓	800	✓	✓	RCD Snubber capacitors
C302, C303	0.47μ	8.4m	0.65n	✓	400	✓	✓	C Snubber capacitors
C301	10μ	9.9m	11n	✓	800	✓	✓	

Note) Refer to Figure 6 for the model composition.
Note) The value is constant unless otherwise specified as ‘Tunable’.

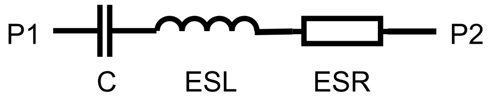

Figure 6. Capacitor Model

Note) We have not been able to confirm operation with all combinations.
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<PCB Pattern Parasitic Inductors>

Table 9. EVK PCB Pattern Parasitic Inductor model

Symbol	Inductor Values			Sim Settings	Symbol	Inductor Values			Sim Settings
	SERL [nH]	SERR [mohm]	Tun-able	Initial Current = 0 Option		SERL [nH]	SERR [mohm]	Tun-able	Initial Current = 0 Option
LP1	1.086	4	✓		LP14	5.58	79	✓	
LP2	0.9024	5	✓		LP15	0.868	2	✓	
LP3	3.914	20	✓		LP16	1.23	4	✓	✓
LP4	3.818	10	✓		LP17	1.255	4	✓	
LP5	1.922	9	✓		LP18	0.7346	2	✓	
LP6	1.598	8	✓		LP19	1.571	4	✓	✓
LP7	1.194	6	✓		LP20	2.481	6	✓	✓
LP8	5.384	25	✓		LP21	2.136	8	✓	
LP9	3.413	90	✓		LP22	4.358	13	✓	
LP10	2.634	12	✓		LP23	3.147	103	✓	
LP11	1.637	33	✓		LP24	3.372	34	✓	
LP12	5.58	16.5	✓		LP25	3.194	83	✓	
LP13	5.58	16.5	✓						

Note) Refer to Figure 7 for the model composition.
Note) The value is constant unless otherwise specified as 'Tunable'.
Note) The inductor models are defined from the analysis of the PCB pattern design data and the accuracy is not guaranteed.

Note) We have not been able to confirm operation with all combinations. Please read the disclaimer carefully.

LP1 through LP25 are PCB pattern inductor models. These are defined from the electro-magnetic analysis of the PCB pattern layout and applied to the simulation circuit as discrete components. Figure 7 shous the model equivalent circuit. The resister of 10 ohm in parallel is for stabilizing simulation.

You can modify these inductors, for example, referring to the layout design constraints to relatively evaluate how the pattern layout would affects the switching behaviors.

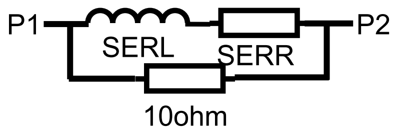

Figure 7. Parasitic L model

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<Analytical Tools>

Analytical tools are used in the simulation circuit for current sensing and device loss calculation.

1. Current Sensing Tool

The component ‘Current to Continuous Quantity’ outputs the current flow ‘p1’ through ‘p2’ (See Figure 8.)
It is used to measure the drain current of the SiC MOSFET.

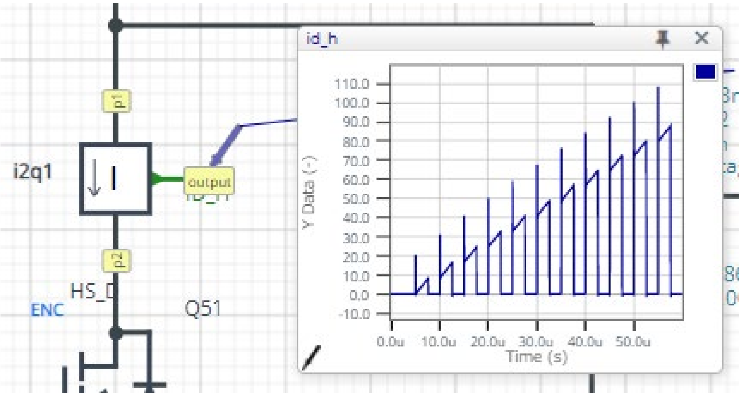

Figure 8. Current to Continuous Quantity

2. Device Loss Calculation Tool

The component ‘Loss_Calc3’ calculates the voltage difference between ‘p1’ and ‘p2’, and outputs the products of the voltage difference and ‘i_sense’ current input as ‘loss_out’ and its integration as ‘loss_integ_out’ (See Figure 9.)

$$loss\_out(t) = \mathrm{v}(t) \times i\_sense(t)$$

$$loss\_integ\_out(t) = \int_0^t loss\_out(t)dt$$

* $\mathrm{v}(t)$: voltage difference between p1 and p2

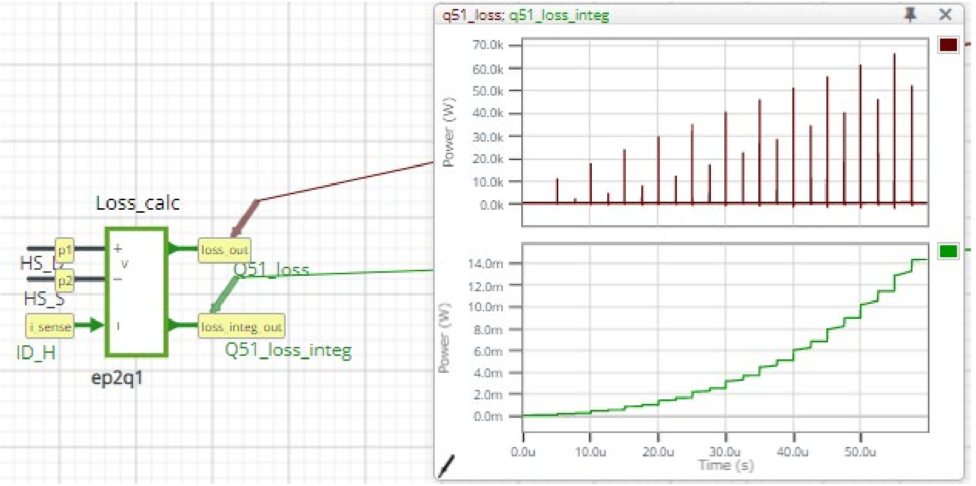

Figure 9. Loss_Calc3

Note) The Loss_calc component is a utility module to support power loss calculation, and does not affect the simulation results of circuit operation or performance.

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