Double Pulse Test Simulation with HB2637L-EVK-301 Simulation Model

2022. Sep
65UG039E Rev.001

<Getting Started>

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How to use ROHM Solution Simulator

Please visit ROHM Solution Simulator page
(https://www.rohm.com/solution-simulator)

- Hands-On User's Manual Link
- Tutorial Short Videos available

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<Outlines>

This simulation circuit provides the double pulse test simulation environment of HB2637L-EVK-301, ROHM's 4th Generation SiC MOSFET Half Bridge Evaluation Board". The simulation circuit is composed of the detailed simulation model with the circuit board parasitic inductance to achieve higher switching waveform simulation accuracy.

Features

- Double pulse test circuit (High-side switching)
- 4th generation SiC MOSFET SCT4036KW7 + gate driver IC BM61S41RFV-C.
- Device equivalent circuit model of the components are used for simulation accuracy.
- Parasitic inductance of PCB patterns are modelled and applied to the simulation circuit.
- Vgs, VDC and other constants can be modified.
- Approx. simulation elapsed time is 6 min.

Applications

- By simulating and verifying the operating conditions and circuit constants of drive circuits, etc., the workload of hardware evaluation can be reduced.
- By extracting the parasitic inductance of the pattern from the PCB layout and adding it to the circuit for simulation, it is possible to improve the problem before prototyping.
- Simulation with the EVK detailed model may help to analyze the cause of noise or surge served in the hardware evaluation.

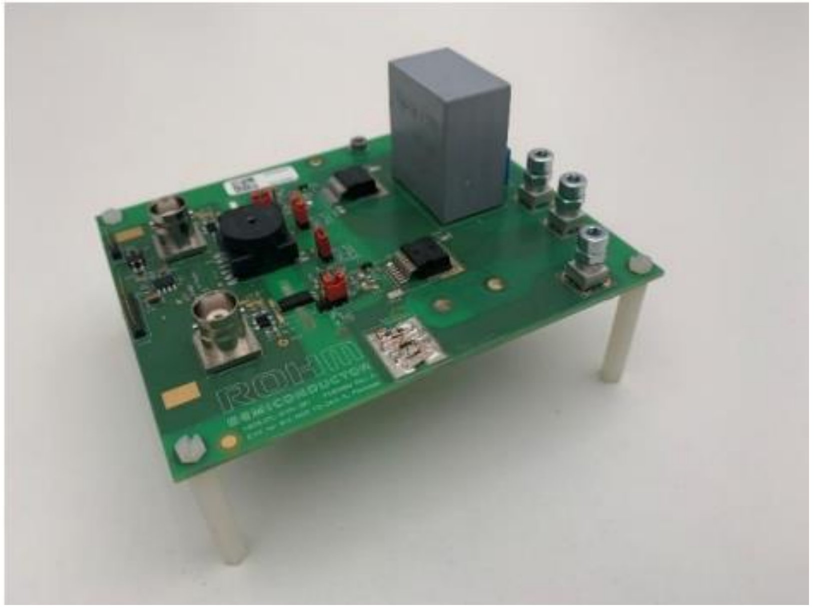

Figure 1. HB2637L-EVK-301

Note) For more details of HB2637L-EVK-301, please refer to the following documents.
HB2637L-EVK-301_ug-e.pdf

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<Simulation Circuit>

Table 1. Parameter Settings

Parameters	Descriptions	Default	Simulation Setting Range
VDC	DC Voltage	800 V	
HS_VCC2, LS_VCC2	Gate drive positive voltage	18 V	15 to 25 V
HS_VEE, LS_VEE	Gate drive negative voltage	0 V	0 to 4 V
Tj	Q51, Q151 Device Junction Temperature	25 °C	
LS_VPULSE	Low-side pulse period	10 μs	Fixed
	Low-side pulse width	4.9 μs	
HS_VPULSE	"L" (DC)		

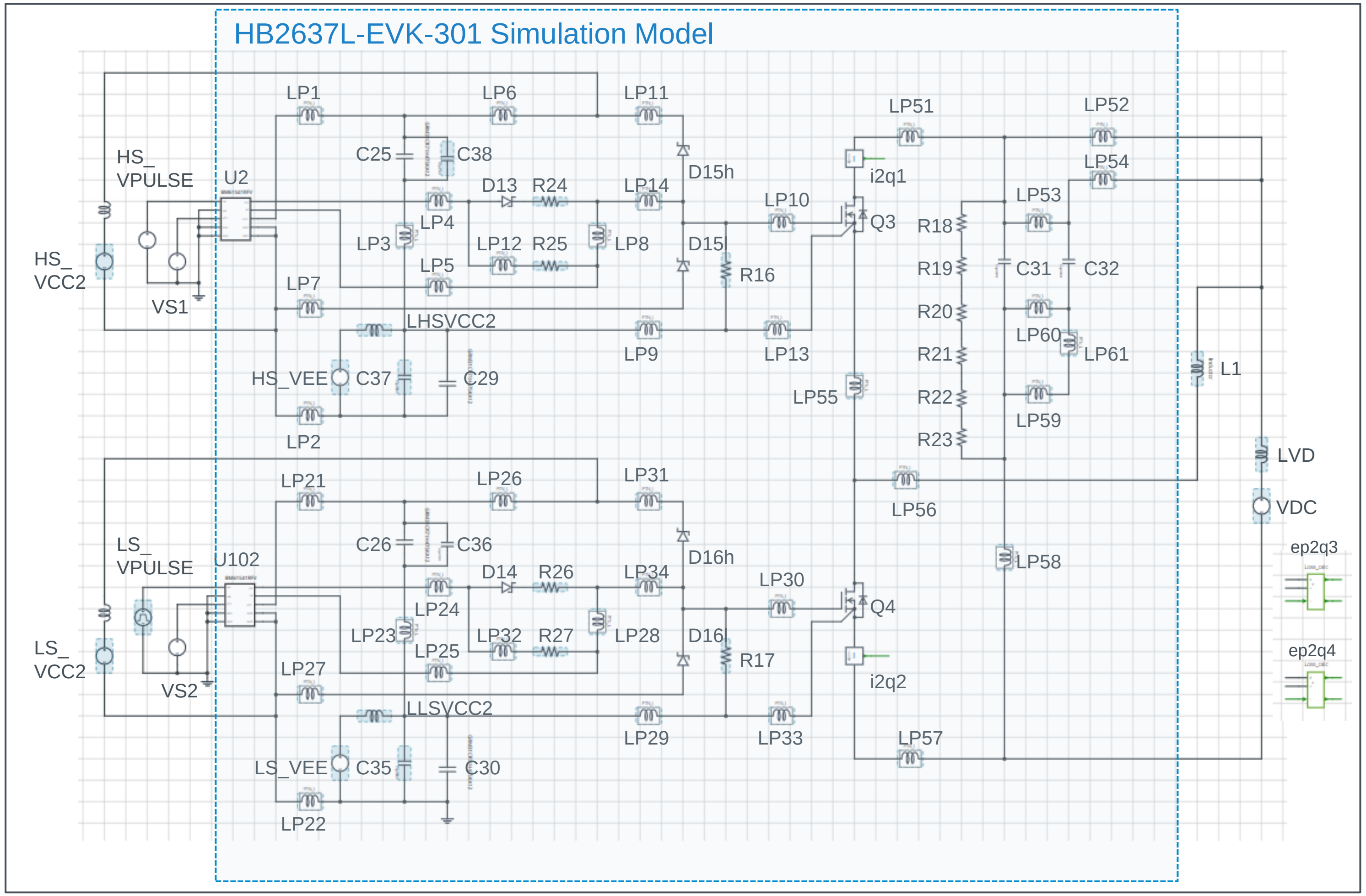

Figure 2. Simulation Circuit

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<Simulation Settings>

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How to setup the gate drive pulse

1. Gate drive voltage Vgs

Figure 3 shows a simplified gate drive circuit, and Figure 4 shows an example of the Vgs waveform. The voltage source VEE gives the voltage of the DS pin of the SiC MOSFET with respect to the VEE2 voltage of the gate driver IC. The voltage source VCC2 gives the supply voltage VCC of the gate driver IC with respect to the voltage reference. As a result, the gate voltage Vgs of the SiC MOSFET is (VCC2-VEE) for 'H' voltage and (-VEE) for 'L' voltage.

Set HS_VCC and HS_VEE for the high-side circuit, and LS_VCC and LS_VEE for the low-side circuit, respectively.

2. Gate Drive Pulse timing

Voltage source 'HS_VPULSE' generate the gate drive pulse timing. The period T = 10μs and the pulse width = 5μs. The actual gate drive pulse output is at the 'out' pin of BM61S41RFV-C, the gate driver IC.

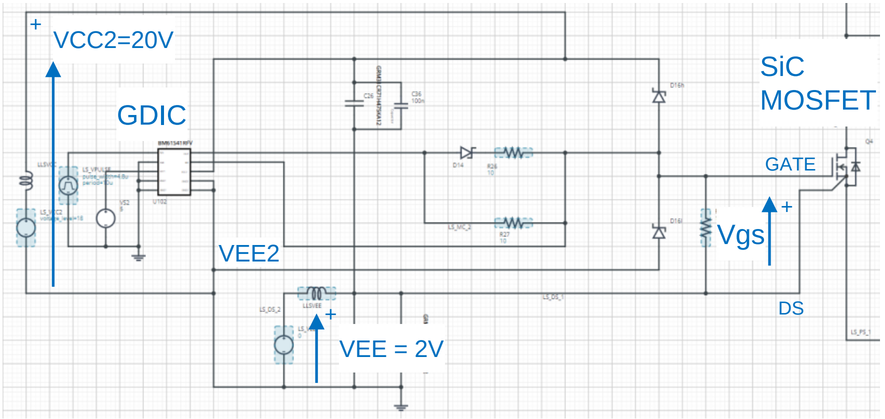

Figure 3. Simplified Gate Drive Circuit
(common for high-side and low-side)

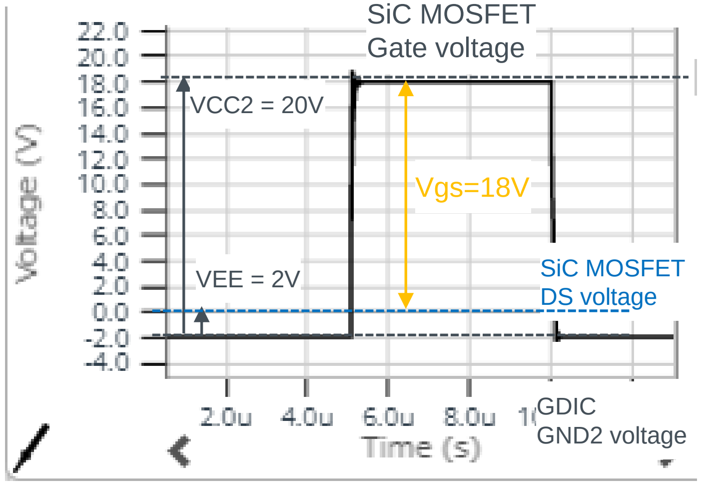

Figure 4. SiC MOSFET Vgs Voltage

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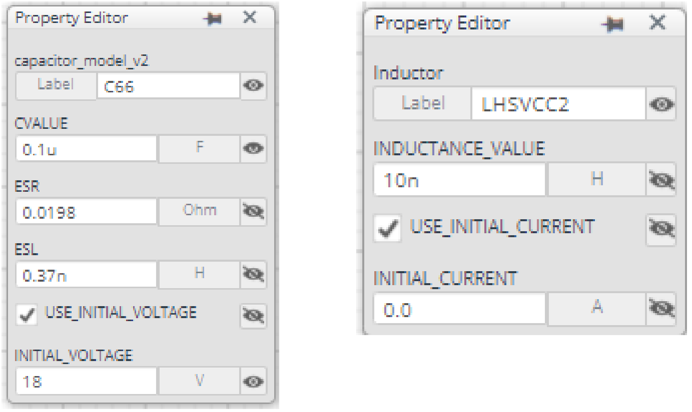
<Simulation Settings>

How to set simulation parameters

1. Using Property Editor

To open the Property Editor, right-click on a component and select "Properties" from the pull-down menu. Figure 5 shows an example of the Property Editor. You can browse the parameters of the component from the Property Editor.

Components shown in blue have “tunable" parameters, and you can change the parameters in the white text box in the Property Editor. Apply the values within the displayed tolerance range.



(a) Capacitor (b) Inductor

Figure 5. Property Editor Examples

2. ‘USE_INITIAL_VOLTAGE’ and ‘USE_INITIAL_CURRENT’

The capacitor property 'USE_INITIAL_VOLTAGE' and the inductor property 'USE_INITIAL_CURRENT' are used to improve simulation convergence and simulation speed. Initial voltage or initial current value will be applied to the component as the initial condition. It will improve simulation convergence. When changing simulation parameters, the initial voltage and the initial current should be revised.
Table 2 and Table3 shows the recommendation of the initial voltage and current.

Table 2. Initial Voltage Recommendation

Symbol	Initial Voltage Recommendation
C38	(HS_VCC2 - HS_VEE)
C37	HS_VEE
C36	(LS_VCC2 - LS_VEE)
C35	LS_VEE

Table 3. Initial Current Recommendation

Symbol	Initial Current Recommendation
L1	0
LHSVCC	0
LLSVCC	0

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<Component List>

Table 4. Power Device / Gate Driver IC Component List

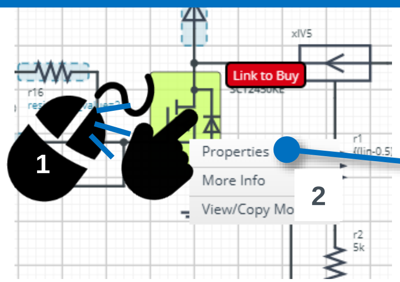
Symbol	Part Number	Device
Q3, Q4	SCT4036KW7	4G-SiC MOSFET, 1200V, 36mohm
D13, D14	RB160MM-40	Schottky Barrier Diode
IC4, IC5	BM61S41RFV-C	1ch Gate Driver Providing Galvanic Isolation
D15(h, l) D16(h, l)	BAT54S	Schottky Barrier Diode

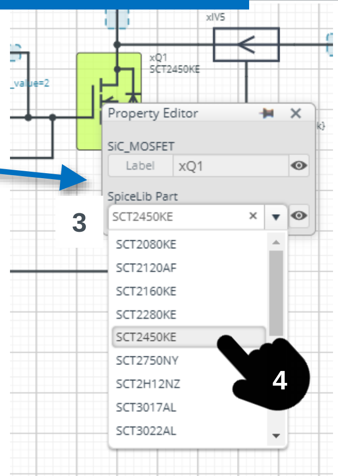
Table 6. Resistor Component List

Symbol	R value [ohm]	Tun-able	Comments
R24, R25, R26, R27	10	✓	Gate resistors
R16, R17	10k	✓	
R18, R19, R20, R21, R22, R23	1M		Bleeder

Note) The value is constant unless otherwise specified as ‘Tunable’.

How to change MOSFET Model





1. Right-click on the device
2. Select “Properties”
3. Pull down “SpiceLib Part”
4. Select the product

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<Component List>

Table 7. Inductor Component List

Symbol	Inductor Values					Simulation Settings	Descriptions
	L [H]	PAR_ RES [ohm]	SER_ RES [ohm]	PAR_ CAP[F]	Tun-able	Use Initial current = 0 Option	
L1	250μ	51k	0.13	2.124p	✓	✓	DPT Inductive Load

Note) Refer to Figure 5 for the model composition.
Note) The value is constant unless otherwise specified as 'Tunable'.

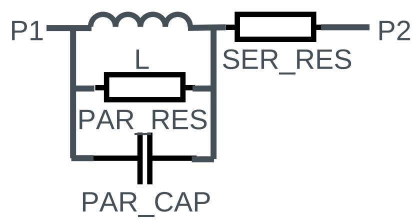

Figure 5. Inductor Model

Table 8. Capacitor Component List

Symbol	Capacitor Values				Simulation Settings		Descriptions
	C [F]	ESR [ohm]	ESL [H]	Tun-able	Initial Voltage [V]	Use Initial Voltage	
C31	5μ	10.9m	27n				
C32	10n	110m	6n				
C36, C38	0.1μ	22.6m	0.4n		18	✓	
C35, C37	0.1μ	22.6m	0.4n				
C25, C26, C29, C30	-	-	-		-		GRM31CR71H475KA12_DC0V_25degC model is used

Figure 6. Capacitor Model

Note) Refer to Figure 6 for the model composition.
Note) The value is constant unless otherwise specified as 'Tunable'.

Note) We have not been able to confirm operation with all combinations.
Please read the disclaimer carefully.

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<PCB Pattern Parasitic Inductors>

Table 9. EVK PCB Pattern Parasitic Inductor model

Symbol	Inductor Values			Sim Settings
	SERL [nH]	SERR [mohm]	Tun-able	Initial Current = 0 Option
LP1	2.326	6	✓	
LP2	0.918	1	✓	
LP3	2.784	2	✓	
LP4	1.570	4	✓	
LP5	5.042	17	✓	
LP6	1.714	5	✓	
LP7	16.82	26	✓	
LP8	0.986	1	✓	
LP9	2.322	1	✓	
LP10	2.089	1	✓	
LP11	3.479	7	✓	
LP12	0.951	1	✓	
LP13	3.880	4	✓	
LP14	1.623	1	✓	
LP21	2.250	6	✓	
LP22	1.115	1	✓	
LP23	2.213	4	✓	
LP24	1.454	4	✓	
LP25	4.841	14	✓	
LP26	1.549	5	✓	

Symbol	Inductor Values			Sim Settings
	SERL [nH]	SERR [mohm]	Tun-able	Initial Current = 0 Option
LP27	15.73	27	✓	
LP28	0.921	1	✓	
LP29	3.133	2	✓	
LP30	1.919	1	✓	
LP31	2.913	7	✓	
LP32	0.913	1	✓	
LP33	4.408	5	✓	
LP34	1.377	1	✓	
LP51	1.154	0.2	✓	
LP52	2.592	1	✓	
LP53	2.038	1	✓	
LP54	1.211	1	✓	
LP55	7.697	2	✓	
LP56	5.289	1	✓	
LP57	29.54	5	✓	
LP58	6.997	1	✓	
LP59	2.298	1	✓	
LP60	2.725	1	✓	
LP61	1.072	0.5	✓	

Table 9 shows the PCB pattern inductor model.
These are defined from the electro-magnetic analysis of the PCB pattern layout and applied to the simulation circuit as discrete components. Figure 7 shous the model equivalent circuit. The resister of 100 ohm in parallel is for stabilizing simulation.

You can modify these inductors, for example, referring to the layout design constraints to relatively evaluate how the pattern layout would affects the switching behaviors.

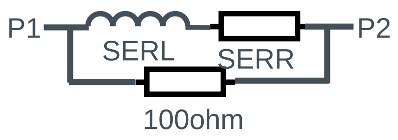

Figure 7. Parasitic L model

Note) Refer to Figure 7 for the model composition.

Note) The value is constant unless otherwise specified as ‘Tunable’.

Note) The inductor models are defined from the analysis of the PCB pattern design data and the accuracy is not guaranteed.

Note) We have not been able to confirm operation with all combinations. Please read the disclaimer carefully.

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<Analytical Tools>

Analytical tools are used in the simulation circuit for current sensing and device loss calculation.

1. Current Sensing Tool

The component 'Current to Continuous Quantity' outputs the current flow 'p1' through 'p2' (See Figure 8.)
It is used to measure the drain current of the SiC MOSFET.

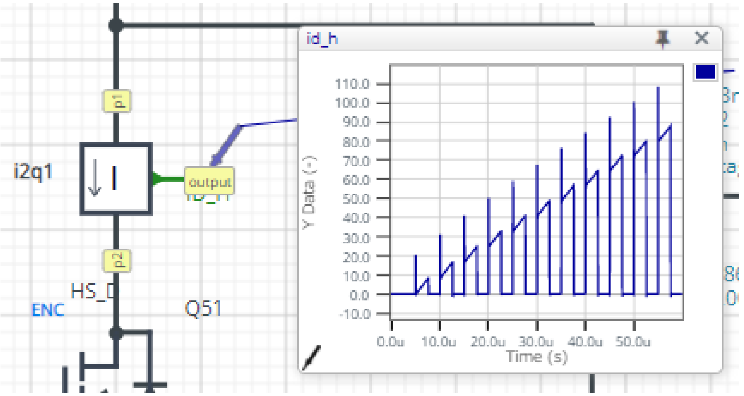

Figure 8. Current to Continuous Quantity

2. Device Loss Calculation Tool

The component 'Loss_Calc3' calculates the voltage difference between 'p1' and 'p2', and outputs the products of the voltage difference and 'i_sense' current input as 'loss_out' and its integration as 'loss_integ_out' (See Figure 9.)

$$loss\_out(t) = \mathrm{v}(t) \times i\_sense(t)$$

$$loss\_integ\_out(t) = \int_0^t loss\_out(t)dt$$

* $\mathrm{v}(t)$: voltage difference between p1 and p2

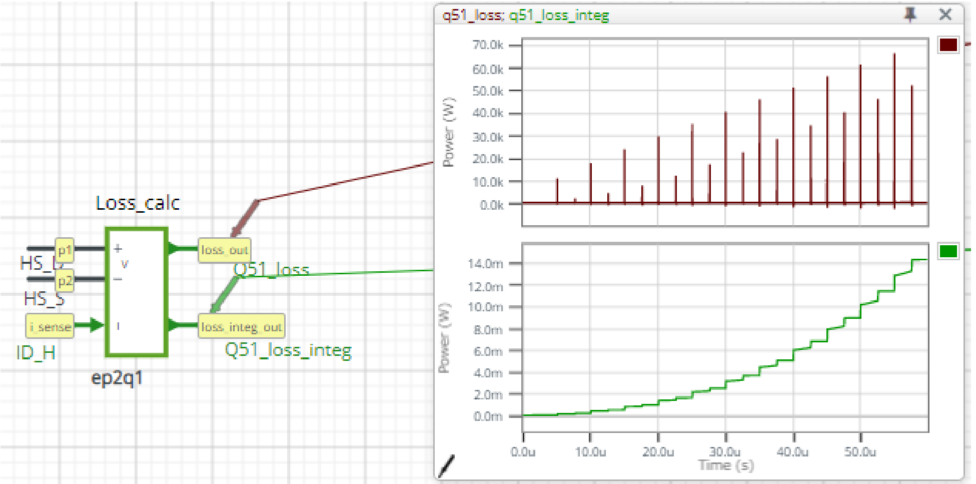

Figure 9. Loss_Calc3

Note) The Loss_calc component is a utility module to support power loss calculation, and does not affect the simulation results of circuit operation or performance.

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