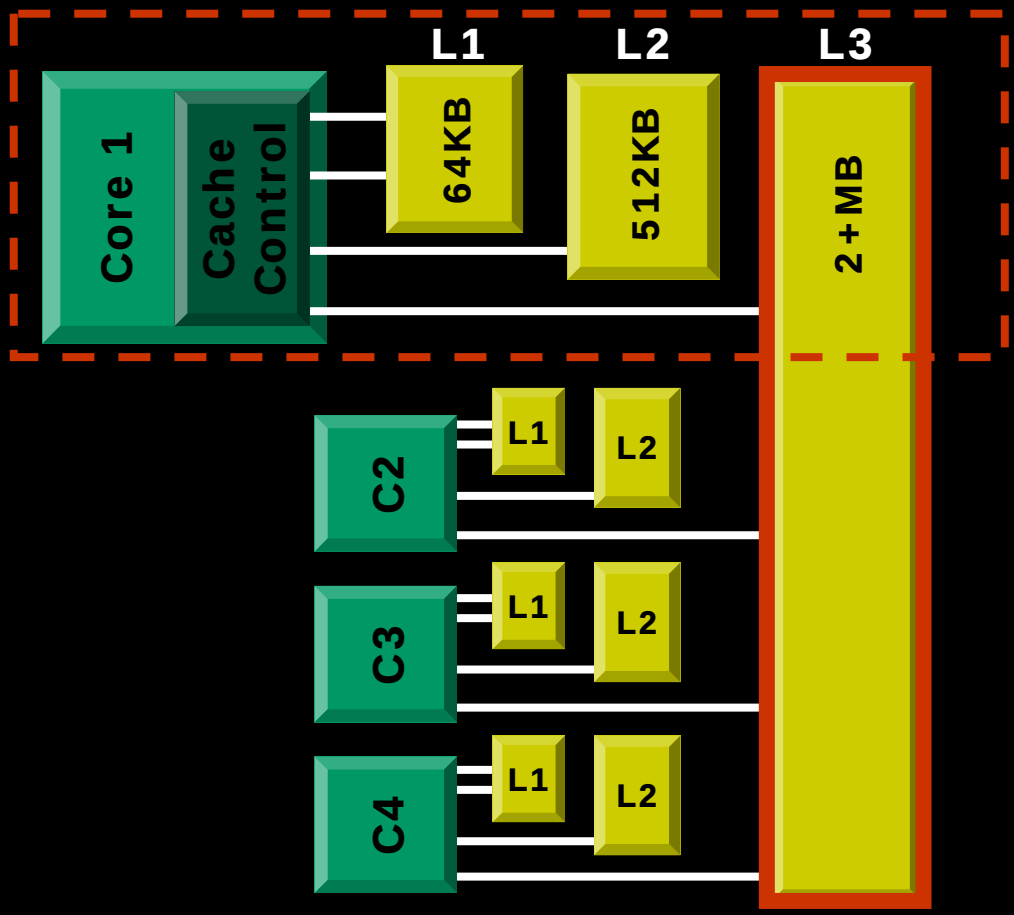
Balanced, Highly Efficient Cache Structure

Superior memory handling reduces the need for "brute force" cache sizes



Shared L3 – *NEW*

- Optimized memory use and allocation for multi-core
- Highly efficient embedded memory controllers allow for appropriate size today
- Ready for expansion at the right time for customers