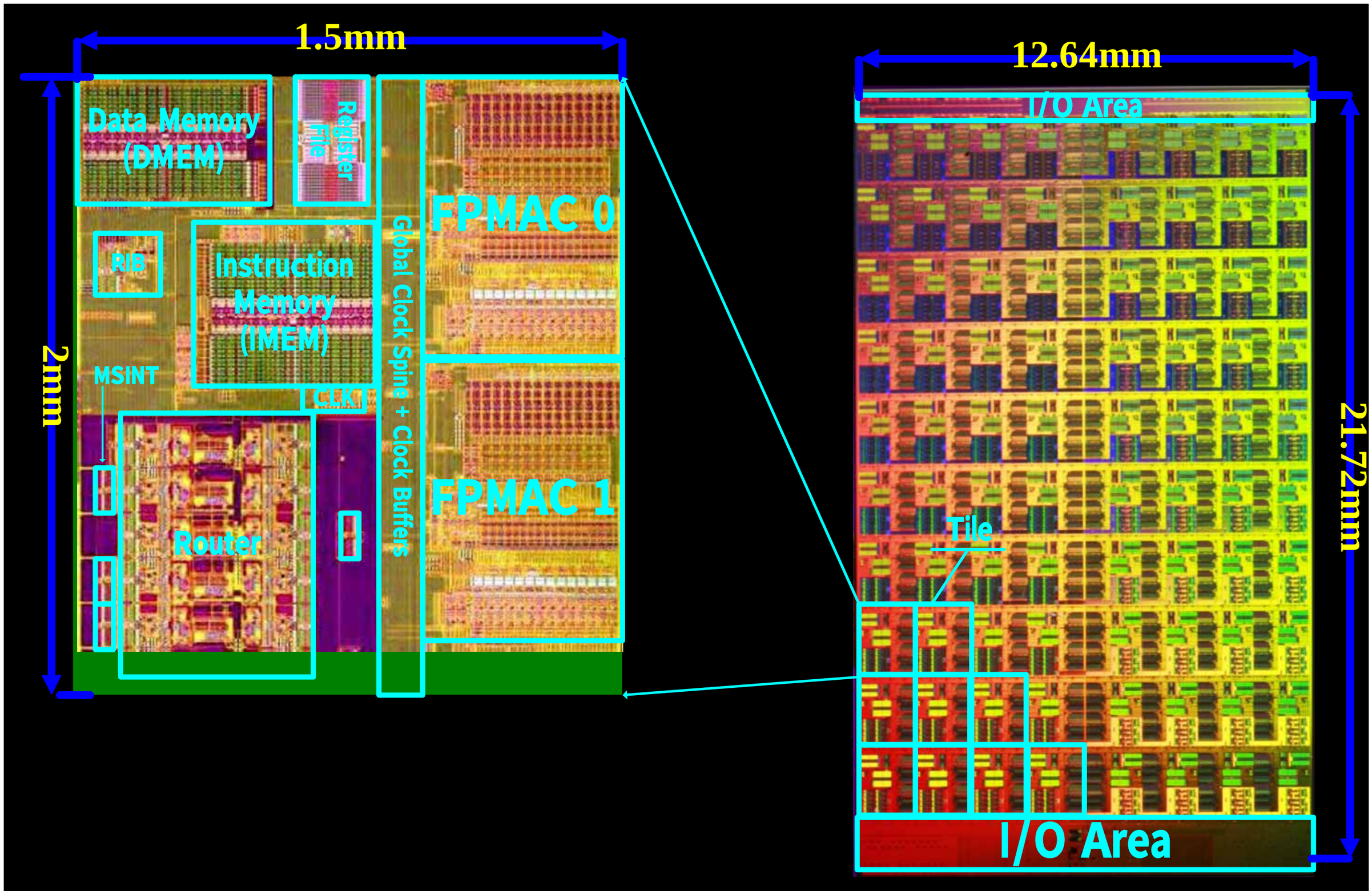
NoC Die Overview



Tile	
Tile Transistors	1.2 M Transistors
Tile Area	3mm2 (1.5mm x 2mm)
Router Transistors	210k Transistors
Router Area	0.34mm2

Full chip	
Process Technology	65nm CMOS
Interconnect	1 poly, 8 metal(Cu)
Transistors	100 M Transistors
Die Area	275mm2 (12.64mm x 21.72mm)
C4 bumps	8390
Package	1248 pin LGA, 14 layers, 343 signal pins