A Delay Model for Interconnect Trees Based on ABCD Matrix

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Abstract - The accuracy of interconnect delay estimations can be improved by the method presented in this paper, in which the first two moments are obtained with ABCD matrix and a stable model to incorporate effects of transport delay into the delay estimate is developed. Simulation results show that the method share the same accuracy with traditional methods when rise time delay is much longer than transport delay and more accurate when the two are of the same order.

I Introduction

Elmore delay model based on RC network, still is one of the most popular interconnect delay estimation tools for circuit synthesis and optimization as well as post layout circuit verification, due to its simplicity, recursive properties and ease of adaptation to VLSI interconnect[1]. Elmore delay model uses the first circuit moment which can not capture the effect of inductance of interconnect, to estimate the delay and the accuracy would be deteriorated when clock frequency increases. To achieve higher accuracy, a two-pole model which based on RLC interconnects is presented by Kahng and Muddu[2]. The model based on the first two moments, gains higher accuracy than previous ones due to the second moment capturing the effect of inductance.

The transmission line in network of the previous models would cut into several segments and replaced with RC or RLC circuits. However, replacing segments with lumped RC or RLC circuits would lead approximation error to calculate the moments. In the paper, transmission line would be replaced with ABCD matrix which can describe the line accurately. And the accuracy of moment calculation would be improved compared to those previous works. Furthermore, the transport delay is ignored in previous models. Therefore, in this paper, the total delay is divided into the transport delay and the rise time delay. The transport delay must be calculated first and remove its impact from the original system. Then, a stable RLC model is used to approximate the new system to estimate the rise time delay.

II. Background

A. Interconnect tree analysis with ABCD matrix

In Kahng's works, each segment of interconnects is modeled as equivalent RLC circuits. The interconnect trees would be replaced with the RLC network. The first moment and the second moment of transfer function from the source to the sink can be easily figured out by iterative formulas[2]. The accuracy of models is mainly dependent on what the number of segment the interconnect lines are cut into. In the paper, each interconnect line is modeled with ABCD matrix. As we all know, the ABCD matrix of interconnects which derive from telegraphy equations can described interconnect accurately.

For an arbitrary interconnect tree, we consider the main path between the source and the sink of interest, and replace each subtree with its respective admittance. To calculate the response at the sink we replace the interconnect line on the main path with ABCD matrix. Fig. 1 shows an example of a main path where every branch on the main path of the tree is replaced with ABCD matrix, and those subtrees off the main path are replaced with their respective admittances. V_n indicates the voltage of node n. V_{N+1} and V_1 indicates the voltage of the source, and the sink respectively. Y_n is the admittance of the node n. $[ABCD]_n$ is ABCD matrix of the interconnect between node n and n+1.

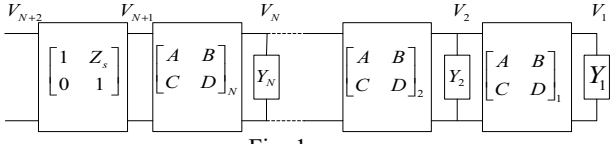

Fig. 1.

To calculate the total transfer function of the ladder network, the transfer function between node n and n+1 should be figured out firstly. For a network described by ABCD matrix as shown in Fig. 2, its transfer function can be easily gotten by formula: $H_n(S) = 1/(A + BY_{n,L})$ (1)

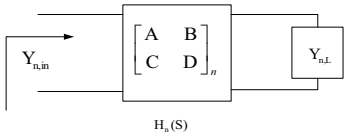

Fig. 2.

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Where $Y_{n,L}$ is the load admittance. To calculate $H_n(S)$, $Y_{n,L}$ the sum of the admittance of subtree and the input admittance of post-order network, must be calculated firstly. So it's necessary to compute the input admittance of the post-order network. $Y_{n,in} = (C + DY_{n,L})/(A + BY_{n,L})$ (2)

$H_n(S)$ is the transfer function between the node n and n+1. $H_s(s)$ is the transform function between the source and the node N+1 . By using formulas (1) and (2), we can get transfer function of each branch. Then the total transfer function from the source to the sink can be given as following: $H(s) = H_s(s)H_N(s)H_{N-1}(s)...H_1(s)$ (3)

B. Classification of delay

The total delay of interconnects is due to the following two components[3]: (I) the transport delay is due to the time taken for the electromagnetic wave to propagate form source to the destination, and (II) interconnect rise time delay is due to the distributed parameters of the interconnect line. The transport delay for an interconnect line of length h is given by $T_{\mathrm{EM}} = h / v$ (4)

Where v is the velocity of electromagnetic wave in transmission line. The rise time delay can be given approximately by following formula.

$$T_{\mathrm{R}} = kRC = krch^2 \quad (5)$$

Where k is constant and R and C are the total resistance and capacitance of the interconnect line.

To the interconnect system with transmission line, the unit step response wave is like curve A as shown in Fig. 3. The total delay of interconnect for given threshold voltage is the sum of T_{EM} and T_R. The previous models ignored T_R would lead big errors when T_{EM} cannot be ignored due to the increasing of the length. As shown in Fig. 3, curve B can hardly match curve A exactly.

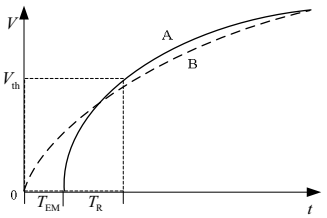

Fig. 3.

III. Analysis of New models

A. Approximation of transfer function

The path from the source to the sink in interconnect tree is regarded as main path, which can be described as a ladder network as shown in Fig. 1. Those interconnect lines on the main path are replaced with ABCD matrix. The ABCD matrix for the transmission line n with length d_n can be obtained by solving the telegraphy equations as following:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_n = \begin{bmatrix} \cosh(\theta_n d_n) & Z_{n,0}\sinh(\theta_n d_n) \\ Y_{n,0}\sinh(\theta_n d_n) & \cosh(\theta_n d_n) \end{bmatrix}$$

Where $Z_{n,o} = \sqrt{(r_n + l_n s)/sc_n}$, $Y_{n,0} = 1/Z_{n,0}$, $\theta_n = \sqrt{(r_n + sl_n)sc_n}$. r_n, l_n and c_n are the resistance, inductance and capacitance per unit length respectively. $Y_{n,L}$ is the load admittance of the line n and its Talyer expansion is as following $Y_{n,L} = y_{n,L}^{(0)} + y_{n,L}^{(1)}s + y_{n,L}^{(2)}s^2 + \ldots$.

We expand the transfer function around s=0, and truncate it by only using the first few coefficient of the expansion. Due to the models in the paper are two order models, only the first three coefficient of the expansion would be used to calculate the transfer function. Additionally, we have $y_{n,L}^{(0)} = 0$ according to the characteristic of the practice circuits [4]. Then we get $Y_L = y_L^{(1)}s + y_L^{(2)}s^2 + \ldots$ (6)

The input admittance $Y_{n,in}$ in the Fig. 2 can be obtained.

$$Y_{n,in} = \frac{C + DY_{n,L}}{A + BY_{n,L}} = \frac{Y_{n,0}\sinh(\theta_n d_n) + \cosh(\theta_n d_n)Y_{n,L}}{\cosh(\theta_n d_n) + Z_{n,0}\sinh(\theta_n d_n)Y_{n,L}}$$

We expand items of the numerator and denominator. Then the first two coefficient of $Y_{n,in}$ can be obtained easily as following $y_{n,in}^{(1)} = C_n + y_{n,L}^{(1)}$

$$y_{n,in}^{(2)} = \frac{R_n C_n^2}{3!} + \frac{y_{n,L}^{(1)} R_n C_n}{2!} + y_{n,L}^{(2)} - (C_n + y_{n,L}^{(1)})(\frac{R_n C_n}{2!} + y_{n,L}^{(1)} R_n) \quad (7)$$

Where $C_n = d_n c_n$, $L_n = d_n l_n$ and $R_n = d_n r_n$

The load admittance of each segment is the sum of the admittance of subtree and the input admittance of post-order segment. So the iterative formula can be given as following

$$Y_{n,L} = Y_n + Y_{n-1,in} \quad (8)$$

When all of $Y_{n,L}$ are figured out by the formula (7) and (8), the transfer function of each segment can be calculated too. According to the formula (1), the transfer function between Y_n and Y_{n+1} is given as following

$$H_n(S) = \frac{1}{\cosh(\theta_n d_n) + Y_{n,L}Z_{n,0}\sinh(\theta_n d_n)} = \frac{1}{1 + h_n^{(1)}s + h_n^{(2)}s^2 + \ldots}$$

The first two coefficients are obtained as following by expanding the each item of the denominator

$$h_n^{(1)} = \frac{R_n C_n}{2!} + y_{n,L}^{(1)} R_n$$

$$h_n^{(2)} = \frac{L_n C_n}{2!} + \frac{(R_n C_n)^2}{4!} + (L_n + \frac{R_n^2 C_n}{3!})y_{n,L}^{(1)} + y_{n,L}^{(2)} R_n \quad (9)$$

$H_s(s)$ is the transfer function between the source and the node N+1. set $Z_s = R_s + sL_s$,

$$H_s(s) = H_{N+1}(s) = \frac{1}{1 + Z_s Y_{N,in}} = \frac{1}{1 + R_s y_{N,in}^{(1)}s + (R_s y_{N,in}^{(2)} + L_s y_{N,in}^{(1)})s^2 + \ldots}$$

Therefore $h_{N+1}^{(1)} = R_s y_{N,in}^{(1)}$, $h_{N+1}^{(2)} = R_s y_{N,in}^{(2)} + L_s y_{N,in}^{(1)}$ (10)

The total transfer function

$$H(s) = H_s(s)H_N(s)H_{N-1}(s)...H_1(s) = \prod_{n=1}^{N+1} H_n(s) \qquad (11)$$

Then the first two coefficients of the total transform function can be obtained as following formula

$$h_1 = \sum_{n=1}^{N+1} h_n^{(1)}, \quad h_2 = \sum_{n=1}^{N+1} h_n^{(2)} + \sum_{n=1}^{N+1} \sum_{\substack{m=1 \\ n \neq m}}^{N+1} h_n^{(1)} h_m^{(1)} \qquad (12)$$

B. The stable model concerned with transport delay

Due to the lumped parameter models can not capture the effect of the transport delay, we divides the delay into two components: the transport delay and the rise time delay. The transport delay of each interconnect segment on the main path between the source and the sink is $T_{f,n} = \sqrt{L_n C_n}$ and can be calculated firstly. Then the total transport delay from the source and the sink is given as following

$$T_f = \sum_{n=1}^{N} T_{f,n} \qquad (13)$$

Since the interconnect system with transmission line is a linear time invariable system, according the feature of transport delay as shown in Fig. 3, we get

$H_n(s) = H_n^*(s)e^{-sT_{f,n}}$, then $H^*_n(s) = H_n(s)e^{sT_{f,n}}$ (14)

Substitute $H_n(s)$ into the formula (11) and expand the numerator and denominator of formula (13) as following

$$H^*(s) = e^{sT_f} \prod_{n=1}^{N+1} H_n(s) = \frac{1 + k_1 s + k_2 s^2 + o(s^2)}{1 + h_1 s + h_2 s^2 + o(s^2)} \qquad (15)$$

Where $k_1 = T_f$; $k_2 = (T_f)^2 / 2$; h_1 and h_2 can be obtained from the formula (10). The first two moments are expressed as following $M_1 = h_1 - k_1$, $M_2 = k_2 - k_1 h_1 + h_1^2 - h_2$ (16)

Due to the resistance of interconnect on chip or MCM have dominate impact on the delay, in the most case we can get[4] M_1 and M_2 are both more than zero. After T_f is removed from $H(s)$, we get the new transfer function $H^*(s)$.

When we use few moments to describe the system, actually the transfer functions are truncated and may lead the instability. So some tactics should be used to deal with the situation. In the paper, we would use a two-order model to approximate $H^*(s)$, which is described as following

$$H_{\text{app}}(s) = (1 + a_1 s)/(1 + b_1 s + b_2 s^2) \qquad (17)$$

Where $a_1 = M_2 / M_1$, $b_1 = M_1 + M_2 / M_1$, $b_2 = M_1^2$.

The first two moments of the new system equal those of $H^*(s)$, besides the stability of the new system can be guaranteed [6]. The two poles $p_{1,2}$ as following are derived from the equation (17). We assume that the input signal is the step signal, and T_R is the rise time delay referring to the threshold voltage V_{th}. Depending on the sign of $b_1^2 - 4b_2$, the poles of the transfer function can be real or complex. We derive delay estimation formulas separately from the two-pole response for each of these cases.

1) Real poles. When $b_1^2 - 4b_2 > 0$, the two-order system has two different poles. The step response is

$$u_{\text{out}}(t) = 1 - \frac{(1 + a_1 p_1) p_2}{p_2 - p_1} e^{p_1 t} + \frac{(1 + a_1 p_2) p_1}{p_2 - p_1} e^{p_2 t} \qquad (18)$$

2) Complex poles. The condition for complex poles is $b_1^2 - 4b_2 < 0$. The step response is

$$u_{\text{out}}(t) = 1 - \frac{\sqrt{\alpha^2 + \beta^2}}{\beta} e^{-\alpha t} \sin(\beta t + \rho) + \frac{a_1(\alpha^2 + \beta^2)}{\beta} e^{-\alpha t} \sin(\beta t) \qquad (19)$$

Where $\rho = \tan^{-1}(\frac{\alpha}{\beta})$ $\alpha = \frac{-b_1}{2(b_2 - a_2)}$

$$\beta = \frac{\sqrt{4(b_2 - a_2) - b_1^2}}{2(b_2 - a_2)}.$$

3) Double poles. The condition for a double pole is $b_1^2 - 4b_2 = 0$. The step response is

$$u_{\text{out}}(t) = 1 - e^{p_1 t} + (p_1 + a_1 p_1^2) t e^{t p_1} \qquad (20)$$

For the given threshold voltage V_{th}, we select the formula (18), (19) or (20) to estimate the rise time delay T_R according to the sign of the $b_1^2 - 4b_2$. In experiments of the paper, we would not use the closed formula to estimate the rise time delay, but calculate the delay directly by match tool MATLAB. $H_{kakng}(s) = 1/(1 + b_1 s + b_2 s^2)$ is used to approximate the transfer function $H(s)$ in Kahng' model, To compare the Kahng model with the new model objectively, the delay would be calculated with MATLAB by using the step response formulas rather than the closed formula derived by Kahng.

IV. Experimental Results and Discussion

A. Example 1

In Fig. 4, a interconnect system with transmission line is shown. $r = 15$ kΩ/m, $l = 246$ nH/m and $c = 176$ pF/m are the resistance, inductance and capacitance per unit length respectively. R_s、L_s、C_T and h are source resistor, source inductor, load capacitor and length of line. Input signal is unit step signal and the delay estimates refer to 50% threshold voltage. In the experiment, simulations would be made by the new model and the Kahng' model separately, and compare those results with those simulated by Hspice which can provide accurate results. In the Table I, the 50% delay of 3mm interconnect line are calculated under the different source impedance and load admittance. In the table 2, the 50% delay at different length are given when $R_s = 50\ \Omega$、$L_s = 2.46$ pH and $C_T = 0.176$ pF.

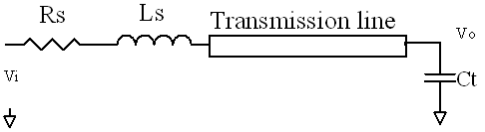

Fig. 4.

TABLE I
50% delay of different source and load

Source		Load	Spice	Delay Model			
				Kahng		New Model	
R_s /Ω	L_s /pH	C_T /pF	/ps	T_d /ps	Error /%	T_{total} /ps	Error /%
40	2.46	0.176	33.9	39.9	17.7	36.3	7.07
50	2.46	0.176	38.9	44.1	15.1	40.6	6.01
75	2.46	0.176	51.9	54.8	5.58	52	0.19
40	2.46	1.76	130	133	2.31	130.7	0.54
50	2.46	1.76	145	148	2.07	145.7	0.48
75	2.46	1.76	184	187	1.63	184.7	0.38

TABLE II
50% delay in different length

h	Spice	Delay Model/ps					
		Kahng		New Model			
		T_d	Error	T_f	T_R	T_{total}	Error
/mm	/ps	/ps	/%	/ps	/ps	/ps	/%
0.1	7.08	7.1	0.28	0.66	6.41	7.07	0.14
0.5	10.5	11.3	7.62	3.29	7.55	10.8	3.33
1	14.9	17	14.1	6.58	9.32	15.9	6.71
1.5	19.9	23.1	16.1	9.87	11.5	21.4	7.39
2	24.4	29.5	20.8	13.2	14.2	27.2	11
2.5	31.6	36.6	15.8	16.4	17.3	33.7	6.64
3	38.3	44.1	15.1	19.7	18.9	40.6	6.01

B. Example2

As shown Fig. 5, the interconnect tree is uniform, and $r = 15$ kΩ/m, $l = 246$ nH/m and $c = 176$ pF/m are the resistance, inductance and capacitance per unit length. The load capacitances of sinks are list in the Table III. The lengths of interconnect line W2, W3, W5, W7 and W8 keep unchanged under different conditions and is 1mm. The rest interconnect lines in the figure are list in the Table II. The delay estimates refer to 50% threshold voltage.

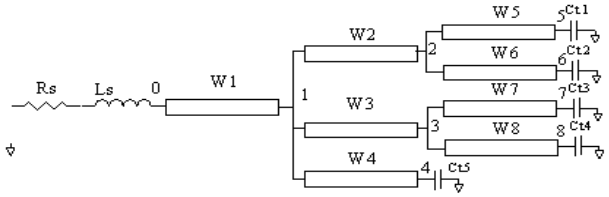

Fig. 5.

TABLE III
50% delay of interconnect trees

Cond.	node /mm	Spice /ps	Delay Model /ps			
			Kahng	New Model		
			Td /ps	T_f /ps	T_R /ps	T_{total} /ps
Cond1	4	120	116	13.2	103.1	116.3
	5	133	137	19.7	115	134.7
	6	150	163	32.9	119	151.9
	7	130	129	19.7	109	128.7
	8	130	129	19.7	109	128.7
Cond2	4	179	201	32.9	154	186.9
	5	180	195	26.3	163	189.3
	6	194	221	39.4	167	206.4
	7	175	188	26.3	158	184.3
	8	175	188	26.3	158	184.3

TABLE IV
The changed parameters under different conditions

Cond.	W1 /mm	W4 /mm	W6 /mm	Ct1 /pf	Ct2 /pf	Ct3 /pf	Ct4 /pf	Ct5 /pf
Cond1	1	1	3	0.176	0.176	0.176	0.176	0.176
Cond2	2	3	3	0.176	0.176	0.176	0.176	0.176

According to the data in the Table I, we can find the model in the paper is more accurate than Kahng's model with the source and load changed when the length of interconnect is large. The main problem of previous lumped parameter models is that their can not capture the transport delay, and the accuracy of estimation would be deteriorated when the transport delay increase, just as shown in the Table II. From the data of the Table II, we can also find that the accuracy of the new model would not deteriorate with the increasing of length as the Kahng's model. The Table III the simulation results of respective nodes of a interconnect tree under different conditions. From the data of the Table III, we can also figure out that when the transport delay and the rise time delay are of same order, the accuracy of estimations would be improved, such as the node 6.

V. Summary and Conclusions

The accuracy of interconnect delay predictions in integrated circuits can be improved by RLC model presented in this paper. In the model, the moments are derived form ABCD matrix firstly. And then the total delay is divided into two components: the transport delay and the rise time delay, to estimate. Simulation results show that the method has the same accuracy with traditional methods when the transport delay is much smaller than the rise time delay and is more accurate when the two are of the same order.

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