# A Tunable Morris-Lecar Spiking Neuron in CMOS

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# A Tunable Morris-Lecar Spiking Neuron in CMOS

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***Abstract*—This article describes a transistor-only tunable Morris-Lecar spiking neuron in CMOS. The tuning of the spiking frequency is accomplished by adjusting the voltage at the body terminal of a reset transistor in a standard 180 nm CMOS process. A tuning sensitivity of 47.85 kHz/V is achieved and can be used to compensate for changes in spiking frequency due to supply voltage variations. The proposed design consumes 1.06 fJ/spike, has a normalized area of 1,549, and has a spiking frequency of 18.37 kHz with a synchronization current of 10 pA.**

## I. Introduction

Neuromorphic chips use spiking neural networks (SNNs) to mimic the human brain. They have emerged as a promising computing architecture for artificial intelligence (AI) and have already been used in applications such as sensing [1], object avoidance [2], and speech recognition [3].

Analog spiking neural network (ASNN) is a subset of SNNs that uses analog circuits [4] to improve its energy efficiency. Recent studies have shown that by biasing transistors in the subthreshold region, the energy efficiency of a simplified Morris-Lecar (ML) neuron (Fig. 1) can be made as low as 1.2 fJ per spike [6]. Furthermore, the area occupied by a simplified Morris-Lecar neuron can be reduced by using a varicap-based design [7] or by removing the on-chip capacitors [8].

One challenge associated with the capacitorless Morris-Lecar neuron is that the spiking frequency ($f_{spike}$) and the energy efficiency ($E_{spike}$) of the spiking neuron are sensitive to variations in supply voltage, temperature, and process variations. *Takaloo et al.* [8] have shown that with 10 % variations in the supply voltage, the spiking frequency can deviate by as much as 33 %. It is therefore desirable to have a neuron implementation that compensates for changes in $f_{spike}$ without changing the synaptic current $I_{syn}$.

It was shown in [9] that the biasing of the body-source junction can be changed to adjust the threshold voltage of MOS transistors in analog circuits. This paper evaluates the feasibility of adjusting $f_{spike}$ by adjusting the body voltages of the reset transistors ($M_3$ and $M_4$ in Fig. 1) and shows that it can be used to compensate for the power supply sensitivity, and to a lesser extent sensitivity to temperature and process variations.

The article is organized as follows: Section II provides the background and simulation results for understanding the operation of a simplified Morris-Lecar neuron. Section III describes the design considerations leading to the tunable transistor-only implementation. Section IV shows the post-layout simulation results. Conclusions are summarized in Sec. V.

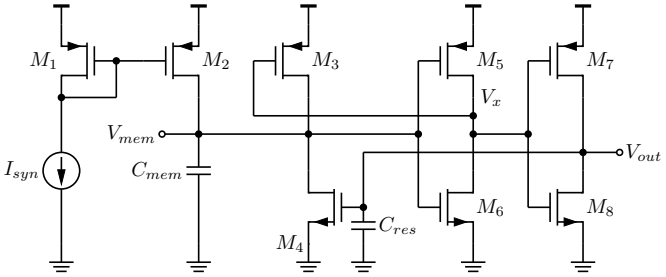



Fig. 1. A simplified spiking neuron based on the Morris-Lecar model [5].

## II. Background

The operation of the simplified Morris-Lecar neuron in Fig. 1 is as follows: $M_1$ and $M_2$ form a 1:1 current mirror. $I_{syn}$ models the movement of neurotransmitters across the synaptic gap. For an initially uncharged $C_{mem}$, $V_{mem}$ is 0 V. $V_x$ is $V_{DDA}$, and $M_3$ is off. $V_{out} = 0$ V and $M_4$ is off. As charges accumulate across $C_{mem}$, $V_{mem}$ increases gradually. $V_{out}$ will increase rapidly once $V_{mem}$ reaches the threshold voltage of the inverter formed by $M_5$ and $M_6$. The falling voltage at $V_x$ momentarily turns on $M_3$. The rising $V_{out}$ momentarily turns on $M_4$ and forces $V_{mem}$ to return to 0 and $V_x$ to rise, turning off $M_3$. $V_{out}$ is returned to 0 V, and a spike is generated. The waveforms of $V_{out}$ and $V_{mem}$ are shown in Fig. 2. $f_{spike}$ is the spike frequency computed from $V_{out}$. And $E_{spike}$ is the energy consumed to generate a spike.

$C_{mem}$ integrates $I_{syn}$. Even though $C_{mem}$ and $C_{res}$ are small (e.g. $C_{mem}$ and $C_{res}$ are 4 fF and 8 fF, respectively, in [5]), they occupy a significant percentage of the area occupied by the neuron (e.g. 65 % of the neuron area in [5]. In 180 nm, $C_g$ is 2 fF/$\mu$m [10], and thus $C_{mem}$ and $C_{res}$ can be implemented using intrinsic gate capacitance and wire capacitance as was done in [8].

## III. Design Considerations

Figure 3 shows the proposed tunable Morris-Lecar spiking neuron. $f_{spike}$ can be adjusted through either $V_{BN}$ or $V_{BP}$. The advantage(s) and the disadvantage(s) of using $V_{BN}$ and $V_{BP}$ to adjust $f_{spike}$ are discussed below.

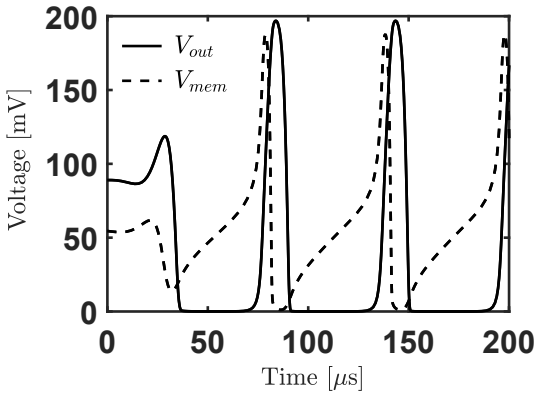



Fig. 2. Waveforms of $V_{mem}$ and $V_{out}$.

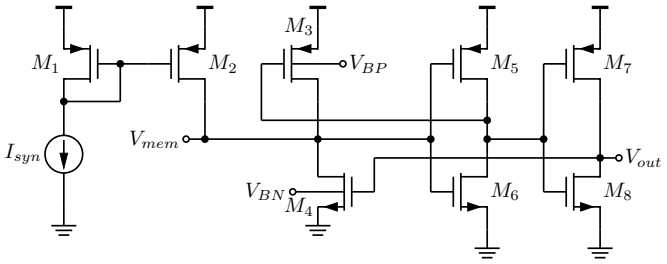
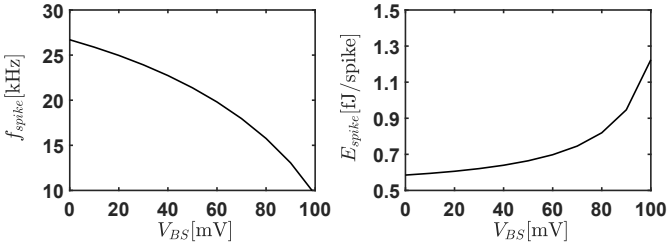



Fig. 3. The proposed tunable Morris-Lecar spiking neuron.

### A. Adjust $f_{spike}$ through $V_{BN}$

Figure 4 shows that the body voltage of $M_4$ can be adjusted to produce a significant change in $f_{spike}$. However, $M_4$ must be placed in a deep $n$-well, which requires a minimum area of $7 \times 8$ $\mu$m$^2$. The layout area of the spiking neuron is thus increased significantly.

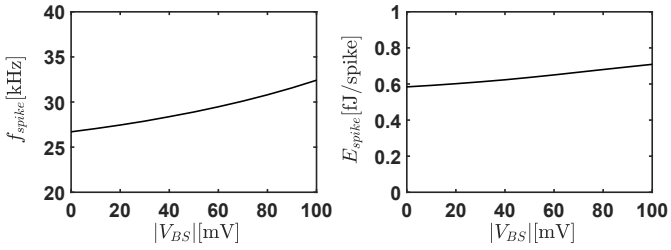



(a) (b)

Fig. 4. (a)$f_{spike}$ and (b) $E_{spike}$ as a function of $V_{BN}$. $V_{BS} = V_{BN}$. $V_{DDA}$, the supply voltage, is 0.2 V. $V_{BP} = V_{DDA}$. $I_{syn} = 10$ pA.

### B. Adjust $f_{spike}$ through $V_{BP}$

Figure 5 shows that the body voltage of a $M_3$ can be adjusted to produce changes in $f_{spike}$. The body terminal of $M_4$ can be connected to ground and does not need to be placed in a dedicated n-well. $M_3$ and $M_4$ can be implemented using regular devices to minimize the active area of the spiking neuron. *It is therefore more desirable to adjust $f_{spike}$ through $V_{BP}$ than through $V_{BN}$.*




(a) (b)

Fig. 5. (a)$f_{spike}$ and (b) $E_{spike}$ as a function of $V_{BP}$. $V_{BN} = 0$ V. $I_{syn} = 10$ pA. $V_{DDA}$, the supply voltage, is 0.2 V. $|V_{BS}|$ is $V_{DDA} - V_{BP}$.

### C. Design Parameters

The parameters of the proposed tunable Morris-Lecar spiking neurons are as follows: $V_{BN}$ **is grounded**. $V_{DDA} = 0.2$ V. $V_{BP}$ is biased nominally at $V_{DDA}/2$ and can be adjusted to change $f_{spike}$. The aspect ratio of $M_1$ and $M_2$ is 1/0.18 $\mu$m/$\mu$m. The aspect ratio of $M_3$, $M_5$, and $M_7$ is 0.44/0.18 $\mu$m/$\mu$m. The aspect ratio of $M_4$ ,$M_6$, and $M_8$ is 0.22/0.18 $\mu$m/$\mu$m. Instead of dedicated capacitors, $C_m$ and $C_{res}$ are implemented using parasitic wire capacitances and intrinsic transistor capacitances to reduce the layout area. Unless otherwise shown, the body terminals of the PMOS transistors are connected to $V_{DDA}$ and the body terminals of the NMOS are connected to 0 V.

## IV. Post-Layout Simulation Results

Figure 6 shows the layout created using Cadence Virtuoso. The parasitics are extracted with Quantus after checking the layout for DRC and LVS violations using Assura.

Figure 7(a) shows that $f_{spike}$ is an increasing function of $I_{syn}$ with $\Delta f_{spike}/\Delta I_{syn}$ equal to 0.9525 kHz/pA at $I_{syn}$=10 pA. $E_{spike}$ is calculated from simulations as discussed in [6] as follows. **First**, the instantaneous current supplied by $V_{DDA}$ is calculated from simulation. **Second**, the instantaneous power consumed is calculated. **Third**, the period of spikes in $V_{out}$ is calculated. **Fourth**, the instantaneous power is integrated over one period of a spike to calculate $E_{spike}$. Figure 7(b) shows that $E_{spike}$ is a function of $I_{syn}$ and has a minimum $E_{spike}$ at $I_{syn}$ =10 pA.

Figure 8 shows that $f_{spike}$ and $E_{spike}$ are both decreasing functions of $V_{BP}$. Setting $V_{BP}$ nominally at $V_{DDA}/2$ (i.e. 0.1 V) allows $f_{spike}$ and $E_{spike}$ to be adjusted as necessary. $\Delta f_{spike}/\Delta V_{BP}$ is -37.3 kHz/V with $V_{BP}$ at $V_{DDA}/2$. The slope of $E_{spike}$ is -2.7 fJ/spike/V with $V_{BP}$ at $V_{DDA}/2$.

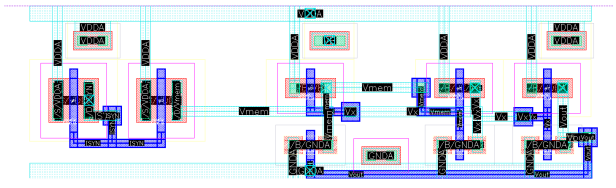
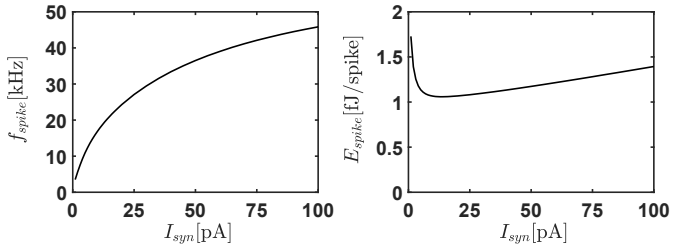
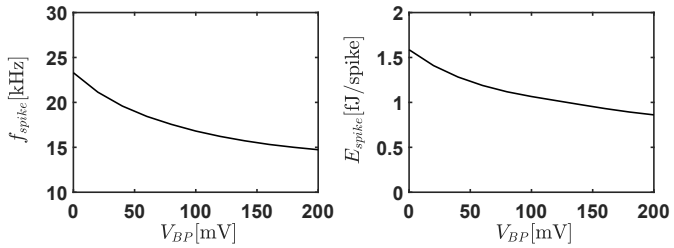


Fig. 6. Physical implementation of the tunable Morris-Lecar neuron. Area is $3.92 \times 12.8$ $\mu$m$^2$.




(a) (b)

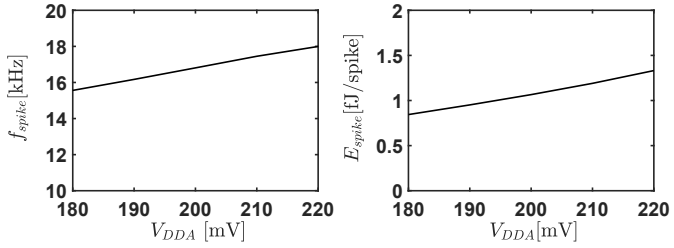
Fig. 7. (a)$f_{spike}$ and (b) $E_{spike}$ as a function of $I_{syn}$. $V_{BP}$ is 100 mV and $V_{DDA}$ is 200 mV. $T$ is 27 $^o$C.




(a) (b)

Fig. 8. (a)$f_{spike}$ and (b) $E_{spike}$ as a function of $V_{BP}$. $I_{syn}$ is 10 pA and $T$ is 27 $^o$C.

Figure 9 shows the supply voltage sensitivities of $f_{spike}$ and $E_{spike}$. The compensation is considered successful if $\Delta f_{spike}$ after compensation is less than $\pm$ 1 % of $f_{spike}$ at the nominal $V_{DDA}$. Table I shows that $V_{BP}$ can be adjusted to compensate for $\pm$10% changes in $V_{DDA}$. Simulations $A$, $B$, and $C$ show that a drop in $V_{DDA}$ by 10% can be compensated by reducing $V_{BP}$ from 100 mV to 65 mV so that $\Delta f_{spike}$ is less than 0.65 %. Simulations $A$, $D$, and $E$ show that an increase in $V_{DDA}$ by 10% can be compensated by increasing $V_{BP}$ from 100 mV to 135 mV so that $\Delta f_{spike}$ is less than 0.1 %.




(a) (b)

Fig. 9. (a)$f_{spike}$ and (b) $E_{spike}$ as a function of $V_{DDA}$. $V_{BP}$=100 mV, $I_{syn}$ = 10 pA, and $T$=27 $^o$C.

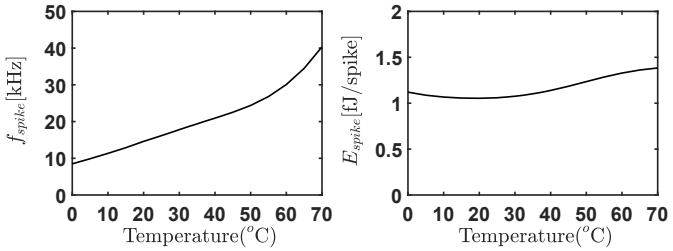
### A. Limitations

*1) Temperature:* Figure 10 shows $f_{spike}$ and $E_{spike}$ between 0 $^o$C and 70 $^o$C–a temperature range for "commercial components" [11]. $f_{spike}$ is an increasing function with a slope equal to 0.312 kHz/$^o$C with $V_{BP}$ at $V_{DD}/2$. Figure 10(b) shows that despite having a complex dependence on $T$, $E_{spike}$ is an increasing function of $T$ for $T > 20$ $^o$C.

Table II shows $V_{BP}$ can be adjusted to provide partial compensation for changes in $T$. Simulations $A$, $B$, and $C$ show

TABLE I
$V_{BP}$ IS ADJUSTED TO COMPENSATE FOR $\pm$10% VARIATIONS OF $V_{DDA}$.

| | Temp. [$^o$C] | $V_{DDA}$ [mV] | $V_{BP}$ [mV] | $I_{syn}$ [pA] | $f_{spike}$ [kHz] | $E_{spike}$ [fJ/spike] |
|---|---|---|---|---|---|---|
| A | 27 | 200 | 100 | 10 | 16.808 | 1.065 |
| B | 27 | 180 | 100 | 10 | 15.561 | 0.844 |
| C | 27 | 180 | 65 | 10 | 16.910 | 0.913 |
| D | 27 | 220 | 100 | 10 | 17.996 | 1.332 |
| E | 27 | 220 | 135 | 10 | 16.809 | 1.235 |




(a) (b)

Fig. 10. (a)$f_{spike}$ and (b) $E_{spike}$ as a function of temperature.

that an increase of $T$ from 27 $^o$C to 43 $^o$C can be compensated by increasing $V_{BP}$ from 100 mV to 180 mV. Simulations $A$, $D$, $E$, and $F$ show that a decrease in $T$ from 27 $^o$C to 0 $^o$C cannot be adequately compensated by reducing $V_{BP}$ to 0 V unless $I_{syn}$ is also increased from 10 pA to 90 pA.

TABLE II
$V_{BP}$ IS ADJUSTED TO PROVIDE PARTIAL COMPENSATION FOR CHANGES IN TEMPERATURE.

| | Temp. [$^o$C] | $V_{DDA}$ [mV] | $V_{BP}$ [mV] | $I_{syn}$ [pA] | $f_{spike}$ [kHz] | $E_{spike}$ [fJ/spike] |
|---|---|---|---|---|---|---|
| A | 27 | 200 | 100 | 10 | 16.808 | 1.065 |
| B | 43 | 200 | 100 | 10 | 21.880 | 1.165 |
| C | 43 | 200 | 180 | 10 | 16.67 | 1.092 |
| D | 0 | 200 | 100 | 10 | 8.490 | 1.120 |
| E | 0 | 200 | 0 | 10 | 9.33 | 1.80 |
| F | 0 | 200 | 200 | 90 | 16.600 | 2.190 |

### B. Process Variations

Figure 11 shows the sensitivities of $f_{spike}$ and $E_{spike}$ to process variations through a Monte Carlo simulation with one thousand samples. The mean value $\mu$ of $f_{spike}$ is 18.37 kHz and the standard deviation $\sigma$ is 6.17 kHz. The mean value of $\mu$ of $E_{spike}$ is 1.06 fJ/spike and the standard of deviation $\sigma$ of $E_{spike}$ is 0.11 fJ/spike. The results indicate that $V_{BP}$ can only provide partial compensation to changes due to process variations.

Figure 12 shows the average peak-to-peak output voltage is 191.25 mV with a $\sigma$ of 14.17 mV and shows that most simulations of $V_{out,pp}$ produce swings greater than $V_{DDA}/2$.

### C. Comparison

Table III shows the comparison of the state of the art. $E_{spike}$ of 1.06 fJ/spike and $f_{spike}$ of 18.37 kHz are obtained via a post-layout Monte Carlo simulation of one thousand samples

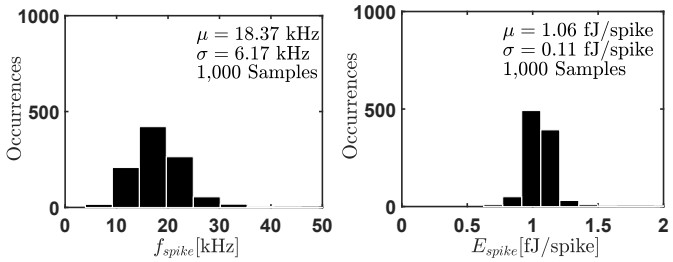



Fig. 11. Monte Carlo Simulations of (a)$f_{spike}$ and (b) $E_{spike}$ with $V_{BP}$ at 0.1 V and $I_{syn}$ at 10 pA.

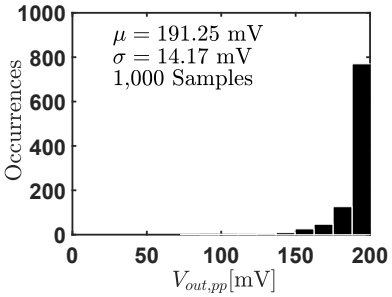



Fig. 12. Monte Carlo Simulations of $V_{out,pp}$ with $V_{BP}$ at 0.1 V and $I_{syn}$ at 10 pA.

with $V_{BP}$ at $V_{DDA}/2$ and $I_{syn}$ at 10 pA. Areas are normalized to $L_{min}^2$ for a technology-independent comparison as proposed by *Takaloo et al.* in [8]. $L_{min}$ is the minimum length in a process. By using intrinsic transistor capacitances and parasitic wire capacitances as state capacitors as discussed in [8], a small normalized area of 1,549 is obtained.

The proposed design minimizes the normalized area through a capacitorless implementation and reduces its sensitivity to supply voltage and temperature variations by adjusting the body voltage of $M_3$ in Fig. 3.

TABLE III
COMPARISON WITH THE STATE-OF-THE-ART MORRIS-LECAR SPIKING NEURON DESIGNS.

| | [6][1] | [8][1] | [7][1] | [5][2] | This work[1] |
|---|---|---|---|---|---|
| $V_{DDA}$ (V) | 0.2 | N/A[5] | -0.1,0.1 | 0.2 | 0.2 |
| Node (nm) | 28 | 45 | 55 | 65 | 180 |
| Area ($\mu$m$^2$) | 34 | 3.91 | 98.6 | 35 | 50.2 |
| Area/$L_{min}^2$ | 39,540 | 1,930 | 32,595 | 8,284 | 1,549 |
| $f_{spike}$ (kHz) | 343 | 6 | 400 | 25 | 18.37 [6] |
| $E_{spike}$ (fJ/spike) | 1.2 | N/A [5] | 1.95 | 4 | 1.06 [6] |
| Tunability[4] | No | No | No | No | Yes |
| $C_m$ (fF) | 3.4 | N/A[3] | varicap | 4 | N/A[3] |
| $C_f$ (fF) | 3.4 | N/A[3] | varicap | 8 | N/A[3] |

[1] Post-layout simulation.
[2] Measurement.
[3] Not applicable. Transistor-only designs.
[4] Tunability is defined as the ability to adjust $f_{spike}$ without changing $I_{syn}$.
[5] Not available.
[6] Obtained through a Monte Carlo simulation of 1,000 samples with $V_{BP}$ at 0.1 V and $I_{syn}$ at 10 pA.

## V. CONCLUSION

This article examines the feasibility of adjusting the spiking frequency of a simplified Morris-Lecar neuron without changing its synaptic current. It was shown that by adjusting the body voltage of the PMOS reset transistor, the spiking frequency can be adjusted to compensate for $\pm 10\%$ change in the supply voltage and provide partial compensation for changes in temperature and process variations. The physical implementation of the design occupies an area of 50.2 $\mu$m$^2$, a normalized area of 1,549, a spiking frequency of 18.37 kHz at 10 pA, and an energy efficiency of 1.06 fJ/spike in post-layout simulations.

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