2. 4GHz 通信モジュール

格 定

品名 2. 4GHz通信モジュール 電源電圧 2.1~3.6V 型名 RM-240 消費電力 送信時:31mA (電流値) 受信時:27mA

電波仕様

周波数帯 2. 4GHz帯 重量 約0.8g

変調方式 DSSS/O-QPSK 外形寸法 16.0mm(縦) × 10.0mm(横) 無線規格 独自規格/IEEE802.15.4準拠

× 3.1mm(厚み) 250kbps

最大転送速度 動作温度 -25°C~+75°C チャンネル数 16ch(2405MHz~2480MHz) 保存温度 -40° C ~ $+85^{\circ}$ C アンテナ チップアンテナ

環境対策 RoHS対応 (モジュール上基板に配線)

セキュリティ 最大送信電力 AES128標準装備 +7dBm(約5mW)

ネットワーク (ソフトにより変更可能) マルチホップ通信標準装備 電波法

工事設計認証取得済 受信感度 -101dBm 最大通信距離 約120m

(見通し距離)

制御仕様

内蔵メモリ

コアプロセッサ 外部I/F STM32W GPIO(24PIN)

(ARM Cortex-M3) $ADC(12bit \times 6ch)$

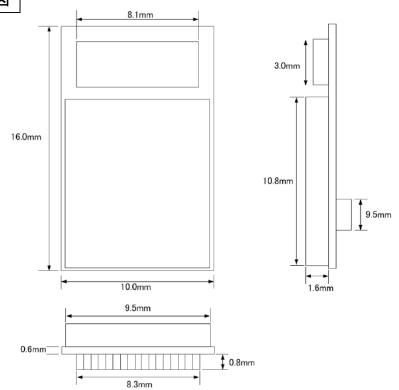
SPI(1ch) Flash: 128KB I2C(1ch) SRAM: 8KB UART(1ch)

> 接続コネクタ 30ピン基板スタックコネクタ(オス)

> > [(502430-3010) Molex製]

Deepスリープ時: 0.8 μ A以下

外形寸法図



퐫 番

RM - 240

GREEN HOUSE

分 類	発 行	頁
RF	2016年2月 (初版)	1/2

2. 4GHz 通信モジュール

ピンアサイン

Pin No	記号	I/O	内容
	PA3	I/O	Digital I/O
	SC2Nssel	I	SPI slave select of Serial Cntroller2
1	TRACECLK	0	Synchronous CPU trace clock
		0	Timer 2 channel 2 output
	TIM2_CH2	I	Timer 2 channel 2 input
	PA4	I/O	Digital I/O
	ADC4	I	ADC Input 4
2	PTI_EN	0	Frame signal of Packet Trace Interface
	TRACEDATA2	0	Synchronous CPU trace data bit 2
	PA5	I/O	Digital I/
	ADC5	I	ADC Input 5
3	PTI_DATA	0	Data signal of Packet Trace Interface
	nBOOTMODE	I	Embedded serial bootloader activation
	TRACEDATA3	0	Synchronous CPU trace data bit 3
	PA2	I/O	Digital I/O
	TIM2_CH4	0	Timer 2 channel 4 output
4		I	Timer 2 channel 4 input
	SC2SCL	I/O	TWI clock of Serial Controller 2
	SC2SCLK	0	SPI master clock of Serial Controller 2
		I	SPI slave clock of Serial Controller 2
_	PA6	I/O	Digital I/O
5	TIM1_CH3	0	Timer 1 channel 3 output
_		I	Timer 1 channel 3 output
6	PB1	I/O	NC Digital I/O
	SC1MISO	0	Digital I/O SDI clave data out of Social Controller 1
	SCIMOSI	0	SPI slave data out of Serial Controller 1 SPI master data out of SerialController1
7	SC1SDA	I/O	TWI data of Serial Controller 1
,	SC1TXD	0	UART transmit data of Serial Controller 1
	SCIND	0	Timer 2 channel 1 output
	TIM2_CH1	I	Timer 2 channel 1 input
Pin No	記号	I/O	内容
Pin No	記号 PB2	I/O	内容 Digital I/O
Pin No		-	
Pin No	PB2	I/O	Digital I/O
Pin No	PB2 SC1MISO	I/O I	Digital I/O SPI master data in of Serial Controller 1
	PB2 SC1MISO SC1MOSI	I/O I I	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1
	PB2 SC1MISO SC1MOSI SC1SCL SC1RXD	I/O I I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1
	PB2 SC1MISO SC1MOSI SC1SCL	I/O I I I/O I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1
8	PB2 SC1MISO SC1MOSI SC1SCL SC1RXD	I/O I I I/O O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output
	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2	I/O I I I/O I O I I I/O I	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input
8	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK	I/O I I I/O I I I/O I I I/O I I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger
8	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK	I/O I I I/O I I I/O I I O I I/O I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG clock input from debugger Digital I/O JTAG data out to debugger
8	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2	I/O I I I/O I I/O I I/O I I/O I I/O I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to
8	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO	I/O I I I I/O I I I O I I/O O O O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger
8	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO	I/O I I I/O I I O I I/O I I/O O I I/O O O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to
9	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3	I/O I I I I/O I I I/O O I I I/O O I I/O O I I/O O I I/O I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger
9	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1	I/O I I I I/O I I I O I I/O O I I/O O I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger
9 10 11	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4	I/O I I I/O I I I/O I I I/O I I I/O I I/O I I/O I I/O I I/O I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger
9 10 11	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS	I/O I I I I	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger
9 10 11	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO	I/O I I I/O I I I/O I I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Serial Wire bidirectional data
9 10 11	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0	I/O I I I/O I I I/O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Serial Wire bidirectional data Digital I/O
9 10 11	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF	I/O I I I/O I I I/O I I I/O I I/O I I/O I I/O O I/O I I/O I I/O O O I/O O O O	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JYAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG mode select from debugger Serial Wire budger Serial Wire budger Serial Wire budger
9 10 11 12	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF VREF	I/O I I I/O I I I/O I I I/O I I/O I I/O I I/O O I/O I I	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG dota in from debugger Serial Wire both in from debugger Serial Wire both in from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input.
9 10 11 12	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTTD1 PC4 JTTMS SWOIO PB0 VREF VREF IRQA	1/O 1 1 1/O 0 1 1 1/O 0 1 1/O 0 1 1/O 0 1 1/O 0 1 1/O 1 1/O 1 1/O 1 1/O 1 1/O 1 1/O 1 1 1/O 1 1 1 1	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A.
9 10 11 12	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF VREF IRQA TRACECLK	1/O 1 1 1/O 0 1 1 1/O 0 1 1/O 0 1 1/O 0 1 1/O 0 1 1/O 1 1/O 1 1/O 1 1/O 0 1 1 1/O 0 0 1 1 0 0	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG mate select from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A. Synchronous CPU trace clock
9 10 11 12	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JITOO SWO PC3 JITD1 PC4 JITMS SWDIO PB0 VREF VREF IRQA TRACECLK TIMICUK	1/O 1 1 1/O 1 1 1 1/O 1 1 1/O 1 1/O 0 1 1/O 0 1 1/O 1 1/O 1 1/O 1 1/O 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Tmer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG made select from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A. Synchronous CPU trace clock Timer 1 external clock input.
9 10 11 12	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF VREF IRQA TRACECLK TIM1CLK	1/O 1 1 1/O 1 1 1 1/O 1 1 1/O 1 1/O 0 1 1/O 0 1 1/O 1 1/O 1 1/O 1 1/O 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Tmer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG mode select from debugger Serial Wire iddirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A. Synchronous CPU trace clock Timer 1 external clock input. Tmer 2 external clock mask input.
9 10 11 12 13	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF VREF IRQA TRACECLK TIM1CLK VDD_PADS	1/O 1 1 1/O 1 1 1 1/O 1 1 1/O 1 1/O 0 1 1/O 0 1 1/O 1 1/O 1 1/O 1 1/O 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG data in from debugger Digital I/O JTAG mode select from debugger Digital I/O JTAG Tombe select from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A. Synchronous CPU trace clock Timer 1 external clock input. Timer 2 external clock mask input. Pads supply (2.1-3.6 V)
9 10 11 12 13 13 14 15	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF VREF IRQA TRACECLK TIMICLK VDD_PADS VDD_PADS	1/O 1 1 1/O 1 1/O 1 1/O 1 1/O 0 1 1/O 1 1/O 1 1/O 1 1 1/O 0 1 1 1/O 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG dock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG mode select from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A. Synchronous CPU trace clock Timer 1 external clock input. Timer 2 external clock mask input. Pads supply (2.1-3.6 V) Pads supply (2.1-3.6 V)
9 10 11 12 13	PB2 SCIMISO SCIMOSI SCISCL SCIRXD TIM2_CH2 SWCLK JTCK PC2 JTDO SWO PC3 JTD1 PC4 JTMS SWDIO PB0 VREF IRQA TIM2CK TIM1CLK TIM1CLK VDD_PADS VDD_PADS PC0	1/O I I I I/O I I I/O I I I/O O I I I/O O I I/O I I I/O I I I/O I I I I	Digital I/O SPI master data in of Serial Controller 1 SPI slave data in of Serial Controller 1 TWI clock of Serial Controller 1 UART receive data of Serial Controller 1 UART receive data of Serial Controller 1 Timer 2 channel 2 output Timer 2 channel 2 input Serial Wire clock I/O with debugger JTAG clock input from debugger Digital I/O JTAG data out to debugger Serial Wire Output asynchronous trace output to debugger Digital I/O JTAG data in from debugger Digital I/O JTAG mode select from debugger Serial Wire bidirectional data Digital I/O ADC reference output. ADC reference input. External interrupt source A. Synchronous CPU trace clock Timer 1 external clock input. Timer 2 external clock mask input. Pads supply (2.1-3.6 V) Pads supply (2.1-3.6 V)

Pin No	記号	I/O	内容
	PC1	I/O	Digital I/O
	ADC3	I	ADC Input 3
17	SWO	0	Serial Wire Output output to debugger
	TRACEDATA0	0	Synchronous CPU trace data bit 0
18	PB7	I/O	Digital I/O
	ADC2	I	ADC Input 2
	IRQC	I	Default external interrupt source C
	TIM1_CH2	0	Timer 1 channel 2 output
		I	Timer 1 channel 2 input
	PB6	I/O	Digital I/O
	ADC1	I	ADC Input 1
19	IRQB	I	External interrupt source B
	TIM1_CH1	0	Timer 1 channel 1 output
	TIMI_CHI	I	Timer 1 channel 1 input
	PB5	I/O	Digital I/O
	ADC0	I	ADC Input 0
20	TIM2CLK	I	Timer 2 external clock input
	TIM1MSK	I	Timer 2 external clock mask input
21			NC
	PC5	I/O	Digital I/O
22	TX_ACTIVE	0	Logic-level control for ext Rx/Tx switch.
23	nRESET	I	Active low chip reset
24	GND		Ground
25	GND		Ground
	PA1	I/O	Digital I/O
	TIM2_CH3	0	Timer 2 channel 3 output
		I	Timer 2 channel 3 input
26	SC2SDA	I/O	TWI data of Serial Controller 2
		0	SPI slave data out of Serial Controller 2
	SC2MISO	I	SPI master data in of Serial Controller 2
Pin No	記号	I/O	内容
	PA7	I/O	Digital I/O
		0	Timer 1 Channel 4 output
27	TIM1_CH4	I	Timer 1 Channel 4 input
	REG_EN	I	External regulator open drain output
	PB3	I/O	Digital I/O
		0	Timer 2 channel 3 output
	TIM2_CH3	I	Timer 2 channel 3 input
28	UART_CTS	I	UART CTS Serial Controller 1
		0	SPI master clock of Serial Controller 1
	SC1SCLK	I	SPI slave clock of Serial Controller 1
29	PB4	I/O	Digital I/O
		0	Timer 2 channel 4 output
	TIM2_CH4	I	Timer 2 channel 4 input
	UART_RTS	0	UART RTS Serial Controller 1
	SC1nSSEL	I	SPI slave select of Serial Controller 1
	PAO	I/O	Digital I/O
	-	0	Timer 2 channel 1 output
30	TIM2_CH1	I	Timer 2 channel 1 input
		0	SPI master data out of Serial Controller 2
	SC2MOSI	I	SPI slave data in of Serial Controller 2
	l		2. 1 3.2. C data in or ochar controller 2

型 番

RM-240

GREEN HOUSE

分 類	発 行	頁
RF	2016年2月 (初版)	2/2