Innovation

Innovation management

With the IoT just around the corner, demand for greater processing power, faster data transfer, lower power consumption, and higher screen resolution continues to increase. Against this backdrop, new semiconductor structures and new material processing technologies are being introduced, prompting the pursuit of innovative memory chips based on new devices and processing technologies that enable further miniaturization. As these issues become increasingly harder to solve with any single piece of processing equipment, semiconductor production equipment manufacturers must offer more comprehensive solutions.

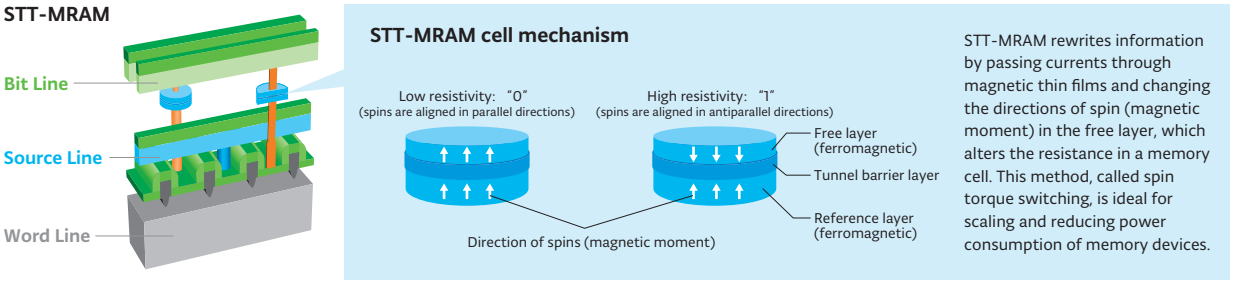
Development of innovative STT-MRAM chip technology

Partnership with Tohoku University

TEL participates in Tohoku University's Center for Innovative Integrated Electronic Systems (CIES) which opened in October 2012, with the goal of accelerating the development of STT-MRAM (Spin-Transfer Torque Magnetoresistive Random Access Memory) manufacturing equipment and chip integration technology.

STT-MRAM is a magnetoresistive random access memory device that uses a data rewrite method called "magnetization reversal induced by spin injection." Being a non-volatile device, it can significantly reduce power consumption, has large capacity and fast data transfer rates, and can rewrite an unlimited number of times. These characteristics are ideal for semiconductor memory.

Using manufacturing equipment developed by TEL, the development of STT-MRAM manufacturing technology has been moving along at an excellent pace. We expect that STT-MRAM device properties will prove suitable for next-generation memory chips in the very near future. Going forward, we intend to apply the research results of the CIES to the development of our own equipment, so we can deliver TEL products that our global customers can rely on in a timely manner.



EXIM™ sputtering system wins Award for Excellence at Semiconductor of the Year 2015

TEL has been developing equipment for manufacturing STT-MRAM, which is attracting attention as an energy-saving memory device. One example is the EXIM™ sputtering system for next-generation semiconductor devices, which won the Award for Excellence in the semiconductor manufacturing equipment category at the Semiconductor of the Year (sponsored by Sangyo Times, Inc.) in June 2015.

The EXIM incorporates advancements in thin film deposition technology, which is considered to be crucial to the manufacture of STT-MRAM, featuring an MR ratio[1] as high as 230%, enabling production of large-capacity memory chips. The EXIM's unique and flexible modular design allows the system to be freely reconfigured for various purposes, ranging from development to mass production.

1 MR (magnetoresistive) ratio: The ratio of the resistance change that occurs when the magnetization directions between free and reference layers switch from parallel state to anti-parallel state, and vice versa. Higher MR ratio is essential for manufacturing large capacity memory devices.

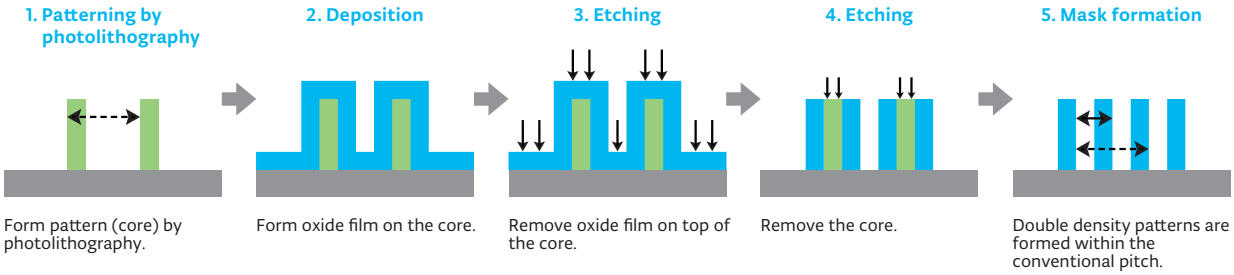
Miniaturization initiatives

Evolution of semiconductors has been driven by miniaturization, which enabled faster processing, less power consumption, and less cost. Now, as the industry is reaching 10nm node, TEL is making extensive efforts to achieve further miniaturization.

In addition to the conventional scaling method that shortens wavelengths of exposure, TEL is applying innovative technologies through the use of process tools, such as film deposition, coating, etching, and cleaning. Self-Aligned Multiple Patterning (SAMP) technology, for instance, forms a film on the sidewalls of an existing pattern to double the patterning density without changing the original pitch. By repeating this process, it further enables the doubling of the pattern density on a chip. TEL is also developing high precision tools for other self-alignment technologies to improve alignment accuracy in multiple patterning processes and improve etch consistency across wafers.

TEL is also conducting joint research and development with IMEC, a world-leading nanoelectronics research institute based in Belgium, to develop advanced patterning technologies. Backed by these efforts, TEL is working to introduce original patterning schemes using new semiconductor structures and materials, and contribute to advancements of miniaturization through our comprehensive process technology expertise.

Self-aligned multiple patterning (SAMP)



Principal systems supporting advanced patterning technology

TELINDY PLUS™ | Tactras™ Vigus™ | Certas LEAGA™ | CLEAN TRACK™ LITHIUS Pro™ Z | CELLESTA™ -i | NS300Z

Protecting and using intellectual property

TEL's fundamental tenet for intellectual property (IP) is to contribute to an increase in corporate revenues by supporting operations in both existing and new market sectors through IP protection. In line with this fundamental direction, TEL allocates IP personnel to product development centers and manufacturing facilities where research and development are performed, as well as to corporate headquarters where its sales and marketing departments are concentrated. These employees work closely with their departments to develop an IP portfolio in line with TEL's technological and product strategies. They also work to minimize the risk of IP disputes by monitoring the competitive environment.

To protect and use IP effectively in regions where TEL and its customers operate, TEL files patent applications in appropriate countries. The global application rate* at TEL has remained at around 70% for five consecutive years. In 2014 its patent application success rates in Japan and in the United States were 78% and 71.2%, respectively.

The strength of this IP portfolio strategy allows TEL to boost revenues by differentiating its products and enhancing its competitiveness.

* Percentage of applications for inventions filed in multiple countries