Feature Article

# Challenge to Technological Innovation

**Dramatic improvement of performance of semiconductors has been achieved with miniaturization and the use of larger wafers. This evolution has been supported by semiconductor production equipment, and Tokyo Electron is committed to taking on challenges for innovative technological development to provide greater value to customers.**

## Innovation Management

### Application-oriented device development

The emergence of smartphones gave rise to a new need for "application-oriented" semiconductor device development, with a focus on functions and performance demanded by users. This development requires not only differentiation in device design, but also diversification of materials and process technology. As a manufacturer of semiconductor production equipment, TEL has addressed all technological possibilities and worked on technological development with a system comprehensively prepared for future technologies. This system includes in-house development and joint development with customers, as well as mid- to long-term cooperation with universities and consortia for promising technologies.

### Taking on challenges for miniaturization and higher performance

With ever-growing demand for further miniaturization and higher performance of semiconductors in recent years, TEL is working on the development of innovative equipment.

We are jointly developing EUV (extreme ultraviolet) exposure technology, which is expected to serve as a next-generation lithography technology, with imec[1] and other global consortia and exposure equipment manufacturers. As for multiple patterning technology, which achieves miniaturization with unique deposition and etching technologies, we are developing a process that focuses on reducing patterning cost, aiming to bring the 10-nanometer node to practical use.

Meanwhile, we are demonstrating the equipment and process technology for 3DI (three-dimensional integration) technology, which allows production of higher performance semiconductors with three-dimensional chip stacking. We accomplish this through process integration evaluation with a consortium.

[1] imec: A world-leading nanoelectronics research center. imec conducts joint research with businesses around the world on technology for information and communications, healthcare, and energy for technological innovation based on scientific knowledge.

ALD System
NT333™
This semi-batch ALD deposition system based on a concept different from the conventional ALD method can achieve high-quality nanoscale deposition while maintaining high productivity.

Metallization System
Trias*e*+™ EX-II™ TiN
This is the latest single wafer metal deposition system for next-generation devices. Featuring low temperature, excellent step coverage, and thin-film controllability, this system can handle various deposition materials.

### High-speed, large-scale data processing and power-saving device development

To achieve the goals of future device development—high-speed, large-scale data processing and power-saving devices—we are conducting research on next-generation semiconductors using new materials that outperform conventional silicon. We are working on commercialization of gallium arsenide (GaAs) for higher-speed processing and graphene for power-saving devices, as well as undertaking research and development of silicon photonics[2] as a communication technology with low power consumption.

As an initiative to achieve lower power consumption with next-generation devices, we are focusing on MRAM and participating in an industry-government-academia joint research program at Tohoku University's Center for Innovative Integrated Electronics Systems (CIES), to which we provided support for construction.

[2] Silicon photonics: Technology for forming integrated circuits on silicon by using photonic devices

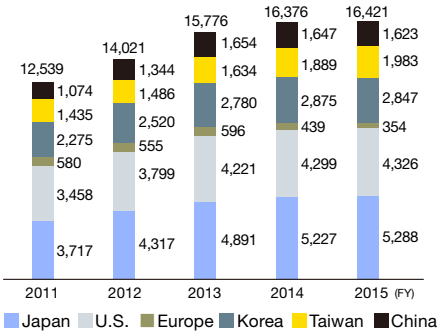
Tohoku University, Center for Innovative Integrated Electronics Systems (CIES)

# Protecting and Using Intellectual Property

## Policy for intellectual property activities

A fundamental tenet of the Tokyo Electron policy for intellectual property (IP) activities is to contribute to an increase in corporate revenues by supporting TEL's business activities in both existing and new market sectors by protecting TEL's IP. With this policy, TEL is developing an IP portfolio to protect its own products in line with its technological and product strategies. Furthermore, TEL fully respects IP rights of third parties. TEL strives to minimize the risk of potential disputes, which could interfere with our business activities, by actively monitoring developments in technology, products, and IP rights, and taking appropriate measures.

### Number of Active Issued Patents




## Operation of intellectual property activities

TEL allocates IP personnel to product development centers and manufacturing facilities, where R&D are performed, as well as to corporate headquarters, where our sales and marketing departments are concentrated, in order to have them work closely with the departments to develop an IP portfolio and minimize the risk of IP disputes. IP personnel also educate engineers and disseminate information to increase awareness and knowledge of IP. In developing the IP portfolio, these personnel organize invention disclosure campaigns and invention mining sessions to ensure R&D achievements be entitled to IP rights. Additionally, for each area of business and R&D, they regularly convene IP committees, composed of IP staff and managers as well as sales/marketing managers and R&D managers. These committees discuss and make decisions about portfolio development and optimization, as well as policies and options for minimizing the risk of IP disputes, in view of market, technological and competitive trends and cost-benefit analyses.

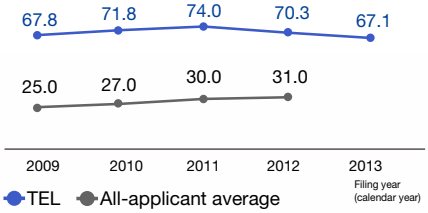
Invention mining session

## Achievements of intellectual property activities

For the protection and effective use of IP in regions where TEL and its customers operate their business, TEL files patent applications not just in Japan but also in other countries. At TEL, the global application rate (percentage of applications for inventions filed in multiple countries) has remained at around 70% for five consecutive years, surpassing by far the average of other Japanese companies. Moreover, TEL fully examines the details and patentability of invention disclosures before filing. Thus, TEL achieved a 74% and 62.8% success rate (or "allowance rate") for applications filed in Japan and in the United States, respectively, in 2013. These figures exceed the average success rates in each country. Additionally, TEL takes low-cost procedures such as direct transaction with local patent firms for filing foreign patent application. Efficient portfolio development with a high success rate and low operating costs is one of the sources of TEL's competitiveness.

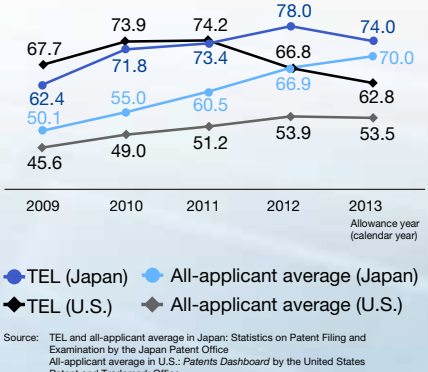
TEL's portfolio contributes not only to the differentiation of its own products and enhancement of its competitive advantage but also to revenue improvement through licensing and selling to other companies.

### Global Application Rate at Japanese Companies




Source: Statistics on Patent Filing and Examination by the Japan Patent Office
* TEL's global application rate in 2013 was compiled by TEL. Japan Patent Office data has not been released.

### Patent Allowance Rate




Source: TEL and all-applicant average in Japan: Statistics on Patent Filing and Examination by the Japan Patent Office
All-applicant average in U.S.: *Patents Dashboard* by the United States Patent and Trademark Office
TEL (U.S.): TEL