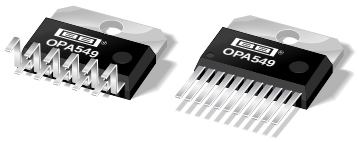
OPA549



SBOS093E – MARCH 1999 – REVISED OCTOBER 2005

High-Voltage, High-Current OPERATIONAL AMPLIFIER

FEATURES

- **HIGH OUTPUT CURRENT:**
  8A Continuous
  10A Peak
- **WIDE POWER-SUPPLY RANGE:**
  Single Supply: +8V to +60V
  Dual Supply: ±4V to ±30V
- **WIDE OUTPUT VOLTAGE SWING**
- **FULLY PROTECTED:**
  Thermal Shutdown
  Adjustable Current Limit
- **OUTPUT DISABLE CONTROL**
- **THERMAL SHUTDOWN INDICATOR**
- **HIGH SLEW RATE: 9V/μs**
- **CONTROL REFERENCE PIN**
- **11-LEAD POWER PACKAGE**

APPLICATIONS

- **VALVE, ACTUATOR DRIVERS**
- **SYNCHRO, SERVO DRIVERS**
- **POWER SUPPLIES**
- **TEST EQUIPMENT**
- **TRANSDUCER EXCITATION**
- **AUDIO POWER AMPLIFIERS**

DESCRIPTION

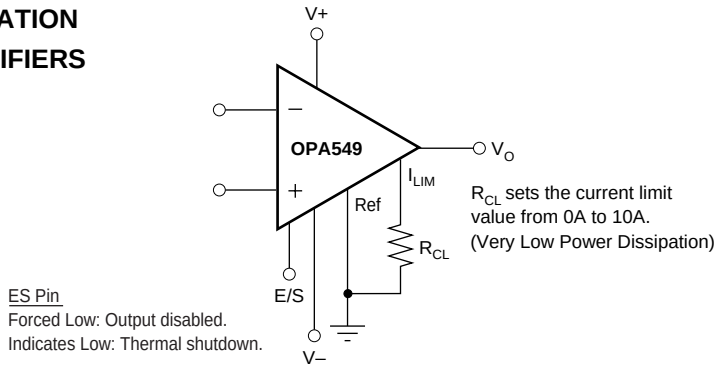
The OPA549 is a low-cost, high-voltage/high-current operational amplifier ideal for driving a wide variety of loads. This laser-trimmed monolithic integrated circuit provides excellent low-level signal accuracy and high output voltage and current.

The OPA549 operates from either single or dual supplies for design flexibility. The input common-mode range extends below the negative supply.

The OPA549 is internally protected against over-temperature conditions and current overloads. In addition, the OPA549 provides an accurate, user-selected current limit. Unlike other designs which use a “power” resistor in series with the output current path, the OPA549 senses the load indirectly. This allows the current limit to be adjusted from 0A to 10A with a resistor/potentiometer, or controlled digitally with a voltage-out or current-out Digital-to-Analog Converter (DAC).

The Enable/Status (E/S) pin provides two functions. It can be monitored to determine if the device is in thermal shutdown, and it can be forced low to disable the output stage and effectively disconnect the load.

The OPA549 is available in an 11-lead power package. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. Operation is specified over the extended industrial temperature range, –40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Output Current	See SOA Curve (Figure 6)
Supply Voltage, V+ to V–	60V
Input Voltage Range	(V–) – 0.5V to (V+) + 0.5V
Input Shutdown Voltage	Ref – 0.5 to V+
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Capability (Human Body Model)	2000V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

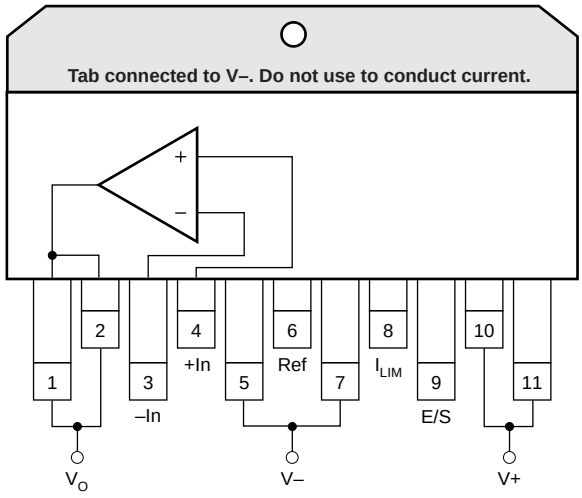
For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet or see the TI website at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

CONNECTION DIAGRAM



Connect both pins 1 and 2 to output.
Connect both pins 5 and 7 to V–.
Connect both pins 10 and 11 to V+.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_{CASE} = +25°C, V_S = ±30V, Ref = 0V, and E/S pin open, unless otherwise noted.

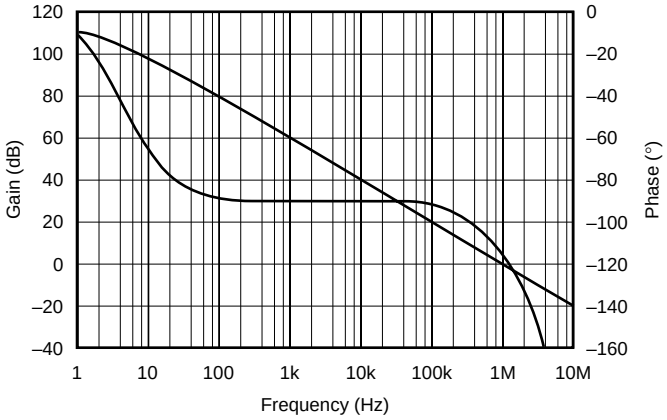
PARAMETER		CONDITION	OPA549T, S MIN	OPA549T, S TYP	OPA549T, S MAX	UNITS
OFFSET VOLTAGE	V_{OS}					
Input Offset Voltage		V_{CM} = 0V, I_O = 0		±1	±5	mV
vs Temperature	**dV_{OS}/dT**	**T_{CASE} = –40°C to +85°C**		**±20**		**µV/°C**
vs Power Supply	PSRR	V_S = ±4V to ±30V, Ref = V–		25	100	µV/V
INPUT BIAS CURRENT(1)						
Input Bias Current(2)	I_B	V_{CM} = 0V		–100	–500	nA
vs Temperature		**T_{CASE} = –40°C to +85°C**		**±0.5**		**nA/°C**
Input Offset Current	I_{OS}	V_{CM} = 0V		±5	±50	nA
NOISE						
Input Voltage Noise Density	e_n	f = 1kHz		70		nV/√Hz
Current Noise Density	i_n	f = 1kHz		1		pA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range: Positive	V_{CM}	Linear Operation	(V+) – 3	(V+) – 2.3		V
Negative	V_{CM}	Linear Operation	(V–) – 0.1	(V–) – 0.2		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = (V–) – 0.1V to (V+) – 3V	80	95		dB
INPUT IMPEDANCE						
Differential				10^7 || 6		Ω || pF
Common-Mode				10^9 || 4		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_O = ±25V, R_L = 1kΩ	100	110		dB
		V_O = ±25V, R_L = 4Ω		100		dB
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBW			0.9		MHz
Slew Rate	SR	G = 1, 50Vp-p Step, R_L = 4Ω		9		V/µs
Full-Power Bandwidth				See Typical Curve		
Settling Time: ±0.1%		G = –10, 50V Step		20		µs
Total Harmonic Distortion + Noise(3)	THD+N	f = 1kHz, R_L = 4Ω, G = +3, Power = 25W		0.015		%
OUTPUT						
Voltage Output, Positive		I_O = 2A	(V+) – 3.2	(V+) – 2.7		V
Negative		I_O = –2A	(V–) + 1.7	(V–) + 1.4		V
Positive		I_O = 8A	(V+) – 4.8	(V+) – 4.3		V
Negative		I_O = –8A	(V–) + 4.6	(V–) + 3.9		V
Negative		R_L = 8Ω to V–	(V–) + 0.3	(V–) + 0.1		V
Maximum Continuous Current Output: dc(4)			±8			A
ac(4)		Waveform Cannot Exceed 10A peak	8			A rms
Output Current Limit						
Current Limit Range				0 to ±10		A
Current Limit Equation				I_{LIM} = 15800 • 4.75V/(7500Ω + R_{CL})		A
Current Limit Tolerance(1)		R_{CL} = 7.5kΩ (I_{LIM} = ±5A), R_L = 4Ω		±200	±500	mA
Capacitive Load Drive (Stable Operation)	C_{LOAD}			See Typical Curve		
Output Disabled						
Leakage Current		Output Disabled, V_O = 0V	–2000	±200	+2000	µA
Output Capacitance		Output Disabled		750		pF
OUTPUT ENABLE/STATUS (E/S) PIN						
Shutdown Input Mode						
$V_{E/S}$ High (output enabled)		E/S Pin Open or Forced High	(Ref) + 2.4			V
$V_{E/S}$ Low (output disabled)		E/S Pin Forced Low			(Ref) + 0.8	V
$I_{E/S}$ High (output enabled)		E/S Pin Indicates High		–50		µA
$I_{E/S}$ Low (output disabled)		E/S Pin Indicates Low		–55		µA
Output Disable Time				1		µs
Output Enable Time				3		µs
Thermal Shutdown Status Output						
Normal Operation		Sourcing 20µA	(Ref) + 2.4	(Ref) + 3.5		V
Thermally Shutdown		Sinking 5µA, T_J > 160°C		(Ref) + 0.2	(Ref) + 0.8	V
Junction Temperature, Shutdown				+160		°C
Reset from Shutdown				+140		°C
Ref (Reference Pin for Control Signals)						
Voltage Range			V–		(V+) – 8	V
Current(2)				–3.5		mA
POWER SUPPLY						
Specified Voltage	V_S			±30		V
Operating Voltage Range, (V+) – (V–)			8		60	V
Quiescent Current	I_Q	I_{LIM} Connected to Ref I_O = 0		±26	±35	mA
Quiescent Current in Shutdown Mode		I_{LIM} Connected to Ref		±6		mA
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range			–40		+125	°C
Storage Range			–55		+125	°C
Thermal Resistance, θ_{JC}				1.4		°C/W
Thermal Resistance, θ_{JA}		No Heat Sink		30		°C/W

NOTES: (1) High-speed test at T_J = +25°C. (2) Positive conventional current is defined as flowing into the terminal. (3) See "Total Harmonic Distortion + Noise vs Frequency" in the Typical Characteristics section for additional power levels. (4) See "Safe Operating Area" (SOA) in the Typical Characteristics section.

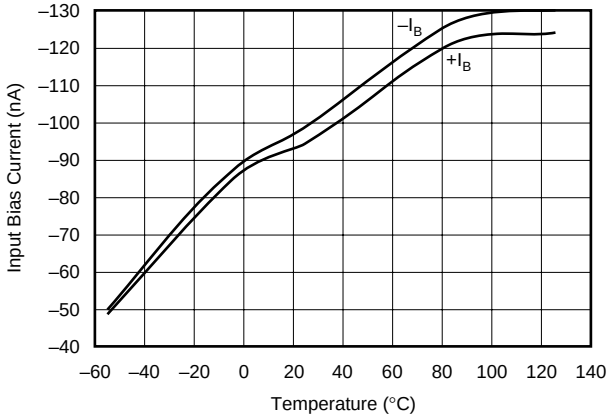
TYPICAL CHARACTERISTICS

At T_{CASE} = +25°C, V_S = ±30V, and E/S pin open, unless otherwise noted.

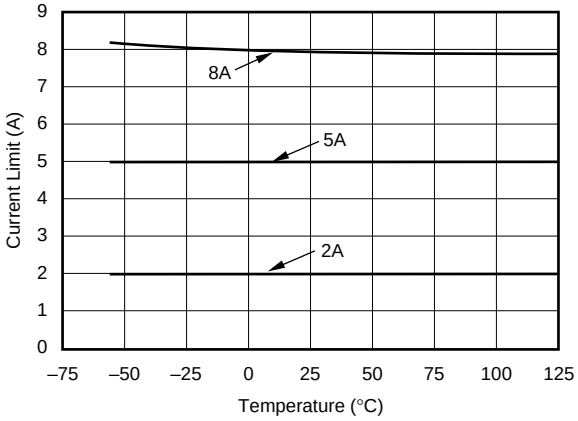
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



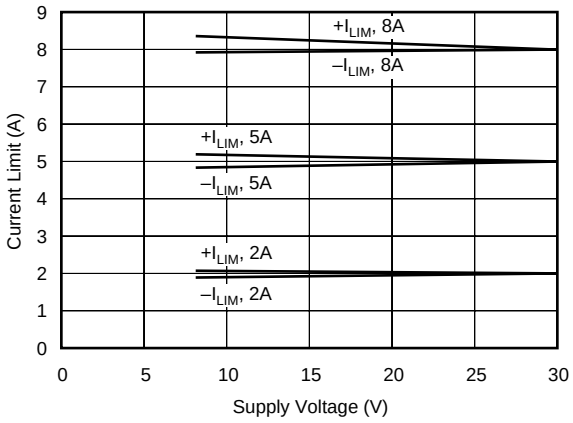
INPUT BIAS CURRENT vs TEMPERATURE



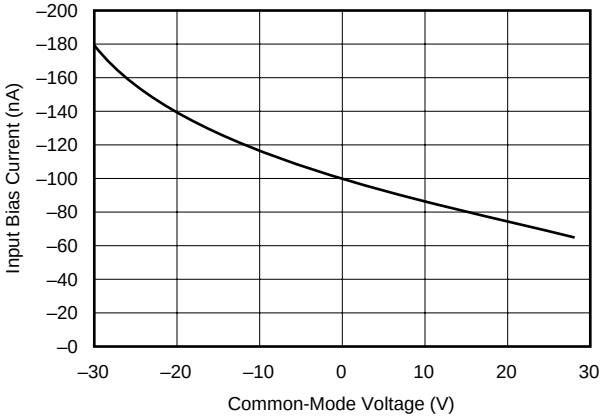
CURRENT LIMIT vs TEMPERATURE



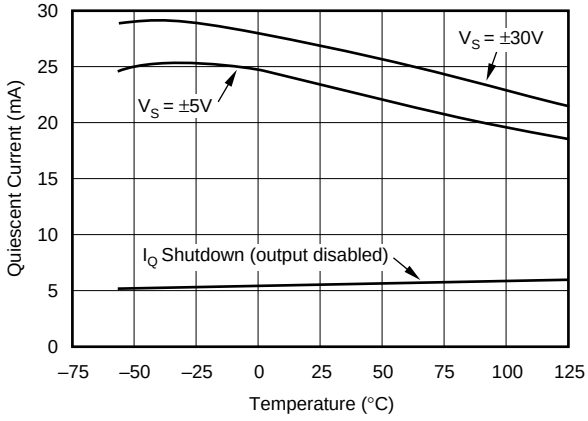
CURRENT LIMIT vs SUPPLY VOLTAGE



INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



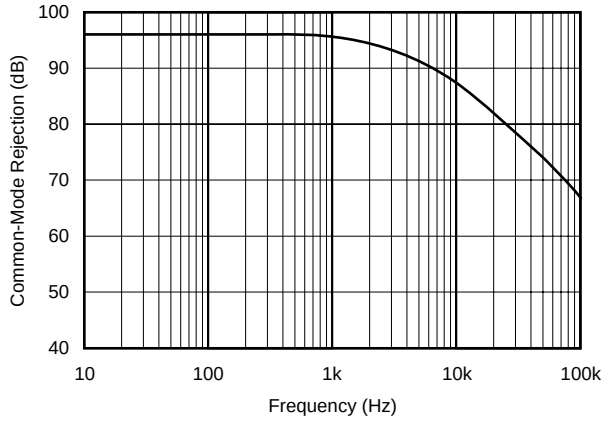
QUIESCENT CURRENT vs TEMPERATURE



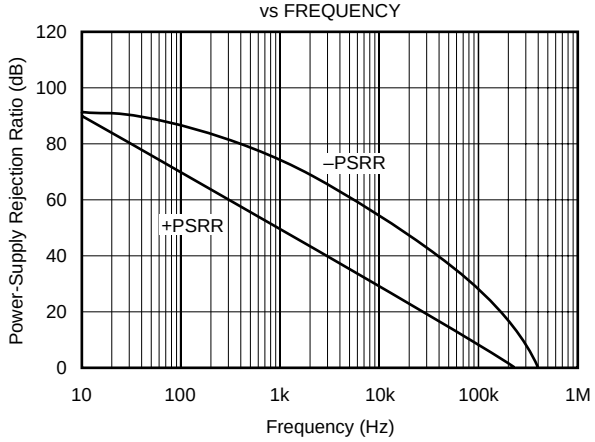
TYPICAL CHARACTERISTICS (Cont.)

At T_{CASE} = +25°C, V_S = ±30V, and E/S pin open, unless otherwise noted.

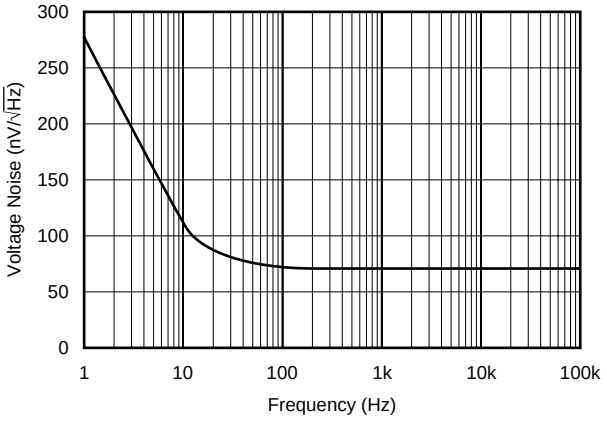
COMMON-MODE REJECTION RATIO vs FREQUENCY



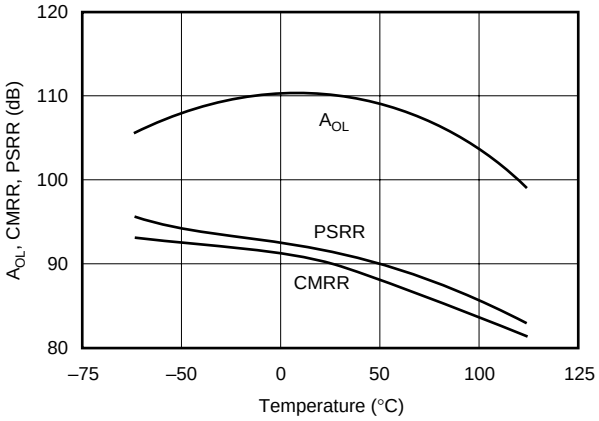
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



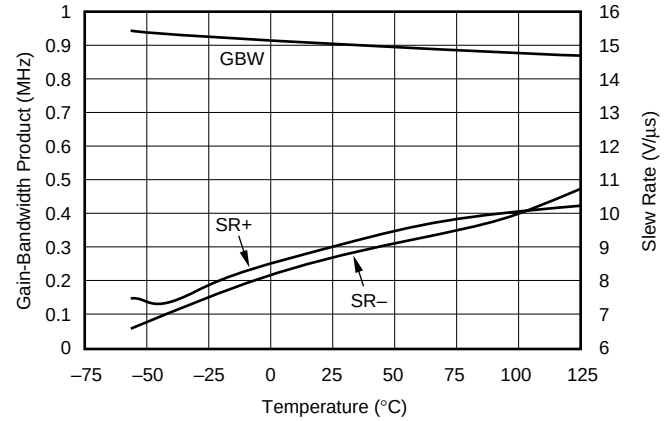
VOLTAGE NOISE DENSITY vs FREQUENCY



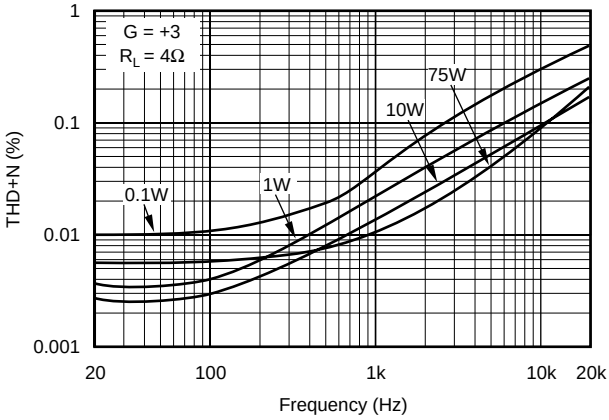
OPEN-LOOP GAIN, COMMON-MODE REJECTION RATIO, AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE



GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE



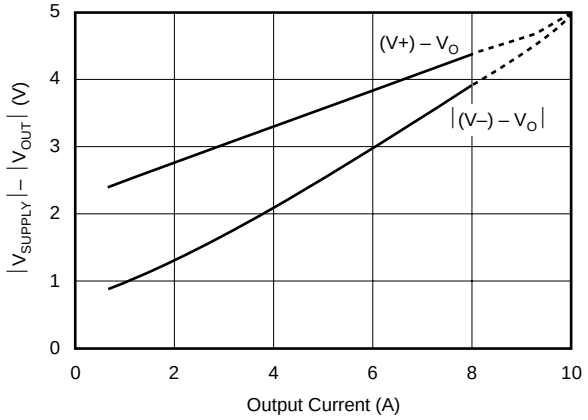
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



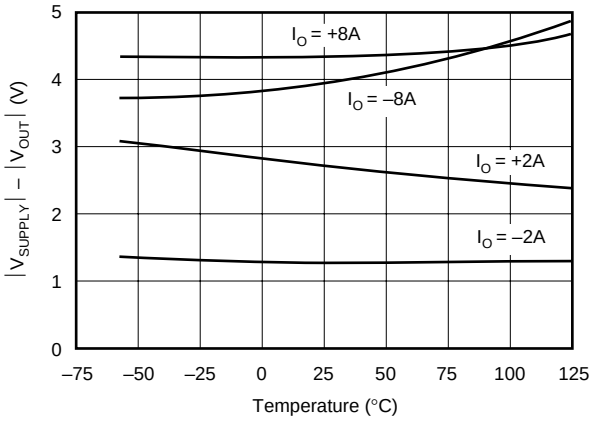
TYPICAL CHARACTERISTICS (Cont.)

At T_{CASE} = +25°C, V_S = ±30V, and E/S pin open, unless otherwise noted.

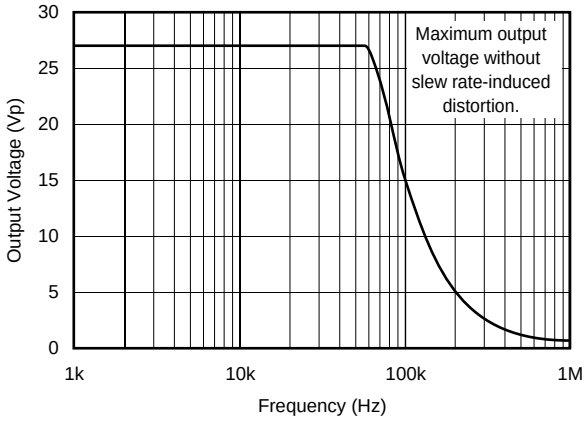
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



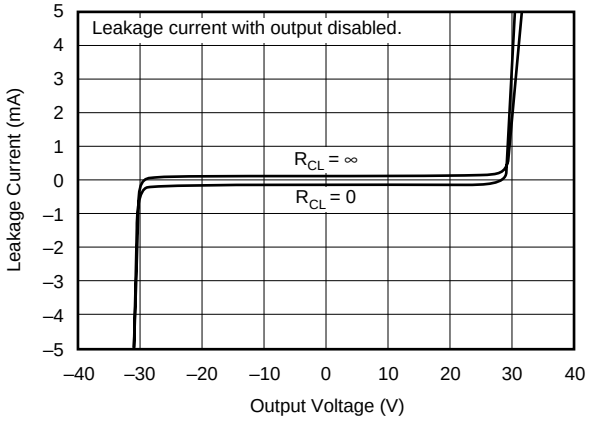
OUTPUT VOLTAGE SWING vs TEMPERATURE



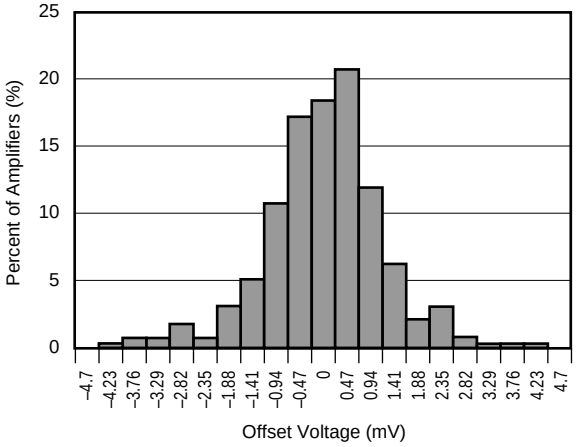
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



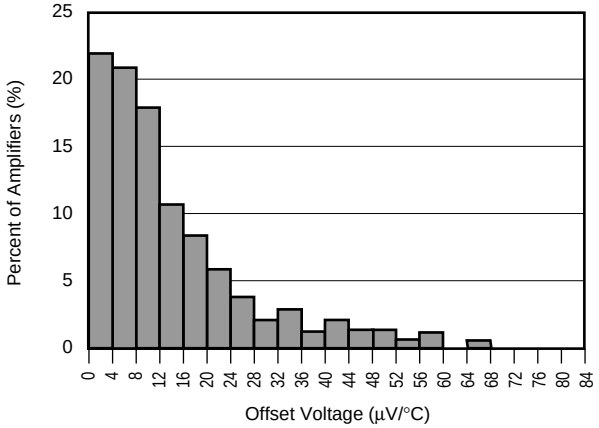
OUTPUT LEAKAGE CURRENT vs APPLIED OUTPUT VOLTAGE



OFFSET VOLTAGE PRODUCTION DISTRIBUTION



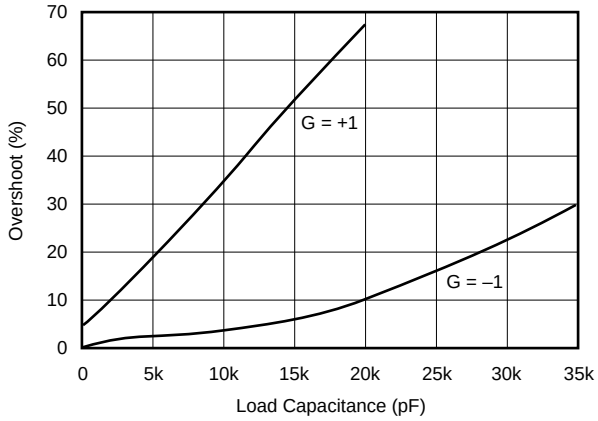
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



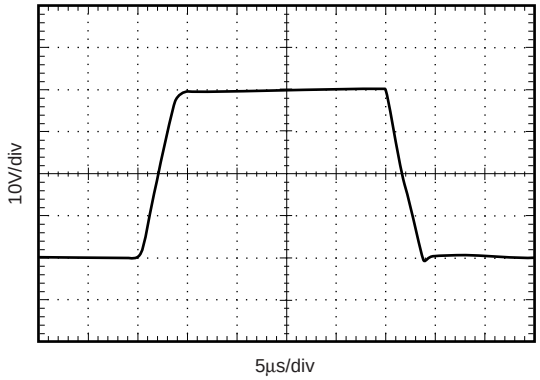
TYPICAL CHARACTERISTICS (Cont.)

At T_{CASE} = +25°C, V_S = ±30V, and E/S pin open, unless otherwise noted.

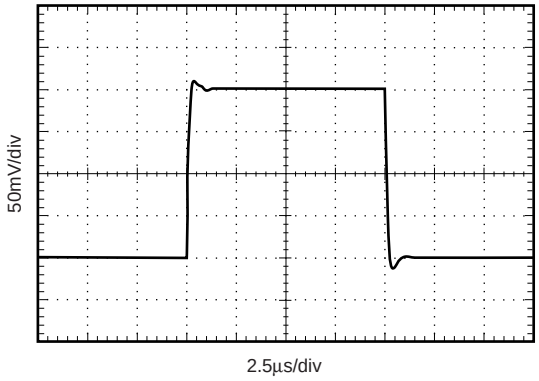
SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



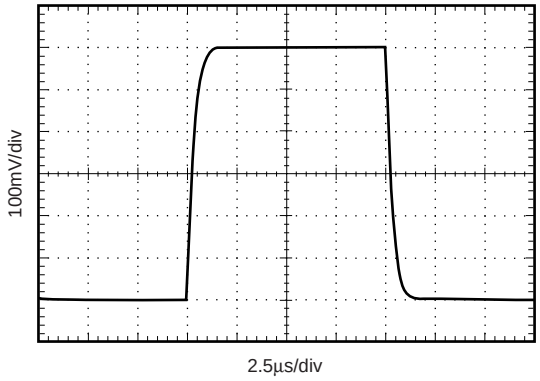
LARGE-SIGNAL STEP RESPONSE
G = 3, C_L = 1000pF



SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 1000pF



SMALL-SIGNAL STEP RESPONSE
G = 3, C_L = 1000pF

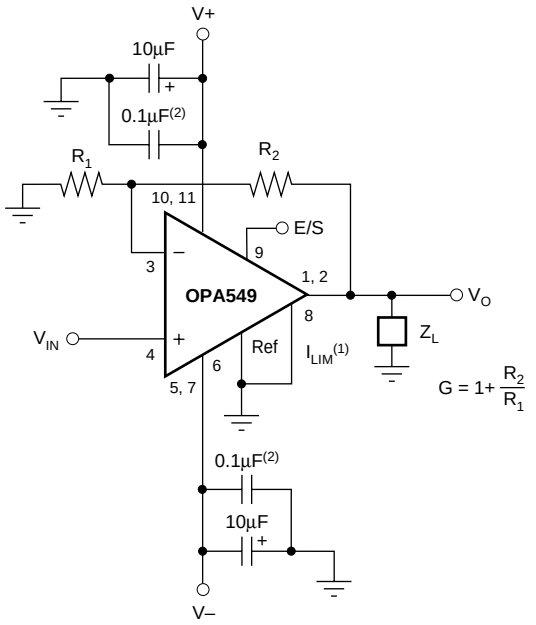


APPLICATIONS INFORMATION

Figure 1 shows the OPA549 connected as a basic noninverting amplifier. The OPA549 can be used in virtually any op amp configuration.

Power-supply terminals should be bypassed with low series impedance capacitors. The technique shown in Figure 1, using a ceramic and tantalum type in parallel, is recommended. Power-supply wiring should have low series impedance.

Be sure to connect *both* output pins (pins 1 and 2).



NOTES: (1) I_{LIM} connected to Ref gives the maximum current limit, 10A (peak). (2) Connect capacitors directly to package power-supply pins.

FIGURE 1. Basic Circuit Connections.

POWER SUPPLIES

The OPA549 operates from single (+8V to +60V) or dual (±4V to ±30V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics. Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA549 can operate with as little as 8V between the supplies and with up to 60V between the supplies. For example, the positive supply could be set to 55V with the negative supply at –5V. **Be sure to connect both V– pins (pins 5 and 7) to the negative power supply, and both V+ pins (pins 10 and 11) to the positive power supply. Package tab is internally connected to V–; however, do not use the tab to conduct current.**

CONTROL REFERENCE (Ref) PIN

The OPA549 features a reference (Ref) pin to which the I_{LIM} and the E/S pin are referred. Ref simply provides a reference point accessible to the user that can be set to V–, ground, or any reference of the user's choice. **Ref cannot be set below the negative supply or above (V+) – 8V. If the minimum V_S is used, Ref must be set at V–.**

ADJUSTABLE CURRENT LIMIT

The OPA549's accurate, user-defined current limit can be set from 0A to 10A by controlling the input to the I_{LIM} pin. Unlike other designs, which use a power resistor in series with the output current path, the OPA549 senses the load indirectly. This allows the current limit to be set with a 0µA to 633µA control signal. In contrast, other designs require a limiting resistor to handle the full output current (up to 10A in this case).

Although the design of the OPA549 allows output currents up to 10A, it is not recommended that the device be operated continuously at that level. The highest rated continuous current capability is 8A. Continuously running the OPA549 at output currents greater than 8A will degrade long-term reliability.

Operation of the OPA549 with current limit less than 1A results in reduced current limit accuracy. Applications requiring lower output current may be better suited to the OPA547 or OPA548.

Resistor-Controlled Current Limit

See Figure 2a for a simplified schematic of the internal circuitry used to set the current limit. Leaving the I_{LIM} pin open programs the output current to zero, while connecting I_{LIM} directly to Ref programs the maximum output current limit, typically 10A.

With the OPA549, the simplest method for adjusting the current limit uses a resistor or potentiometer connected between the I_{LIM} pin and Ref according to Equation 1:

$$R_{CL} = \frac{75kV}{I_{LIM}} - 7.5k\Omega \quad (1)$$

Refer to Figure 2 for commonly used values.

Digitally-Controlled Current Limit

The low-level control signal (0µA to 633µA) also allows the current limit to be digitally controlled by setting either a current (I_{SET}) or voltage (V_{SET}). The output current I_{LIM} can be adjusted by varying I_{SET} according to Equation 2:

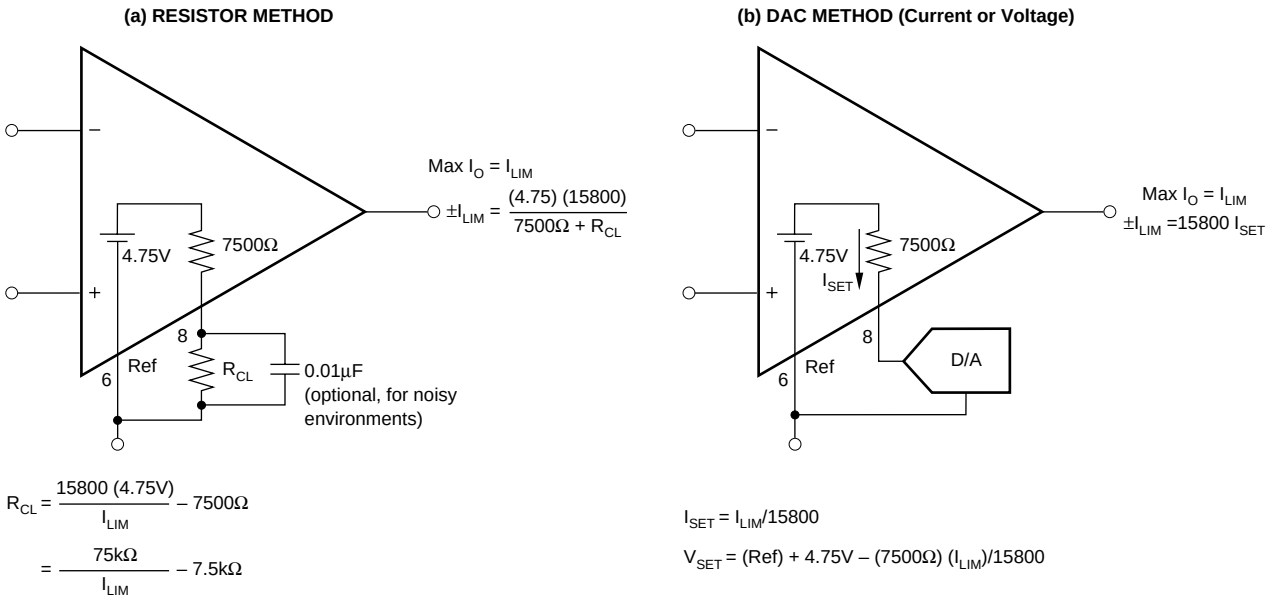
$$I_{SET} = I_{LIM}/15800 \quad (2)$$

Figure 2b demonstrates a circuit configuration implementing this feature.

The output current I_{LIM} can be adjusted by varying V_{SET} according to Equation 3:

$$V_{SET} = (Ref) + 4.75V - (7500W)(I_{LIM})/15800 \quad (3)$$

Figure 11 demonstrates a circuit configuration implementing this feature.



$$R_{CL} = \frac{15800\ (4.75V)}{I_{LIM}} - 7500\Omega$$

$$= \frac{75k\Omega}{I_{LIM}} - 7.5k\Omega$$

$$I_{SET} = I_{LIM}/15800$$

$$V_{SET} = (Ref) + 4.75V - (7500\Omega)\ (I_{LIM})/15800$$

OPA549 CURRENT LIMIT: 0A to 10A

DESIRED CURRENT LIMIT	RESISTOR[1] (R_{CL})	CURRENT (I_{SET})	VOLTAGE (V_{SET})
0A[2]	I_{LIM} Open	0µA	(Ref) + 4.75V
2.5A	22.6kΩ	158µA	(Ref) + 3.56V
3A	17.4kΩ	190µA	(Ref) + 3.33V
4A	11.3kΩ	253µA	(Ref) + 2.85V
5A	7.5kΩ	316µA	(Ref) + 2.38V
6A	4.99kΩ	380µA	(Ref) + 1.90V
7A	3.24kΩ	443µA	(Ref) + 1.43V
8A	1.87kΩ	506µA	(Ref) + 0.95V
9A	845Ω	570µA	(Ref) + 0.48V
10A	I_{LIM} Connected to Ref	633µA	(Ref)

NOTES: (1) Resistors are nearest standard 1% values. (2) Offset in the current limit circuitry may introduce approximately ±0.25A variation at low current limit values.

FIGURE 2. Adjustable Current Limit.

ENABLE/STATUS (E/S) PIN

The Enable/Status Pin provides two unique functions: 1) output disable by forcing the pin low, and 2) thermal shutdown indication by monitoring the voltage level at the pin. Either or both of these functions can be utilized in an application. For normal operation (output enabled), the E/S pin can be left open or driven high (at least 2.4V above Ref). A small value capacitor connected between the E/S pin and C_{REF} may be required for noisy applications.

Output Disable

To disable the output, the E/S pin is pulled to a logic low (no greater than 0.8V above Ref). Typically the output is shut down in 1µs. To return the output to an enabled state, the E/S pin should be disconnected (open) or pulled to at least 2.4V above Ref. It should be noted that driving the E/S pin high (output enabled) *does not defeat internal thermal shutdown*; however, it does prevent the user from monitoring the thermal shutdown status. Figure 3 shows an example implementing this function.

This function not only conserves power during idle periods (quiescent current drops to approximately 6mA) but also allows multiplexing in multi-channel applications. See Figure 12 for two

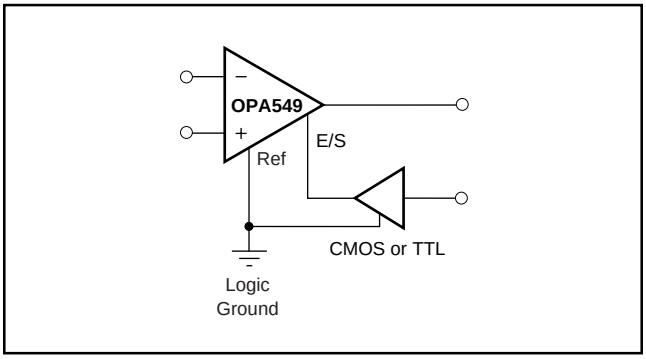


FIGURE 3. Output Disable.

OPA549s in a switched amplifier configuration. The on/off state of the two amplifiers is controlled by the voltage on the E/S pin. Under these conditions, the disabled device will behave like a 750pF load. Slewing faster than 3V/µs will cause leakage current to rapidly increase in devices that are disabled, and will contribute additional load. At high temperature (125°C), the slewing threshold drops to approximately 2V/µs. Input signals must be limited to avoid excessive slewing in multiplexed applications.

Thermal Shutdown Status

The OPA549 has thermal shutdown circuitry that protects the amplifier from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C and allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. The E/S pin can be monitored to determine if the device is in shutdown. During normal operation, the voltage on the E/S pin is typically 3.5V above Ref. Once shutdown has occurred, this voltage drops to approximately 200mV above Ref. Figure 4 shows an example implementing this function.

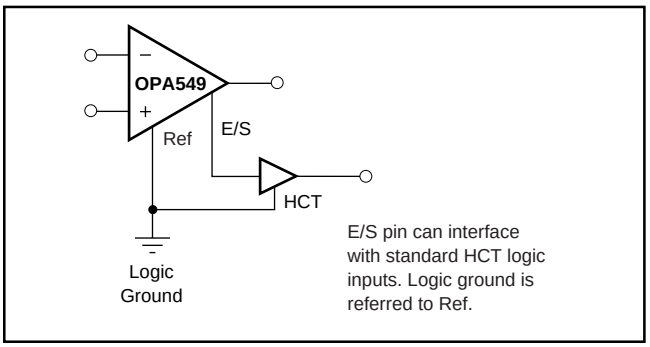


FIGURE 4. Thermal Shutdown Status.

External logic circuitry or an LED can be used to indicate if the output has been thermally shutdown, see Figure 10.

Output Disable and Thermal Shutdown Status

As mentioned earlier, the OPA549's output can be disabled and the disable status can be monitored simultaneously. Figure 5 provides an example of interfacing to the E/S pin.

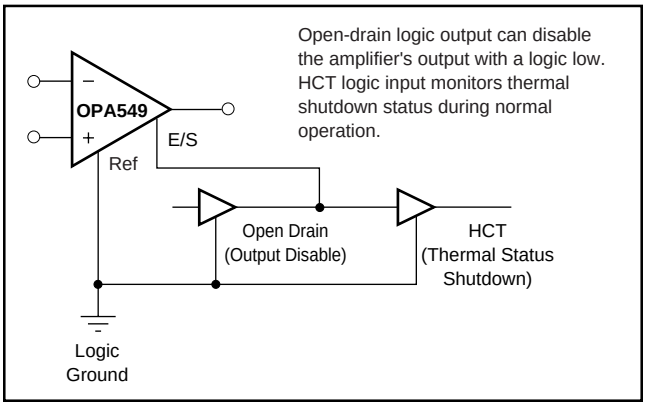


FIGURE 5. Output Disable and Thermal Shutdown Status.

SAFE OPERATING AREA

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistor, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figure 6) shows the permissible range of voltage and current.

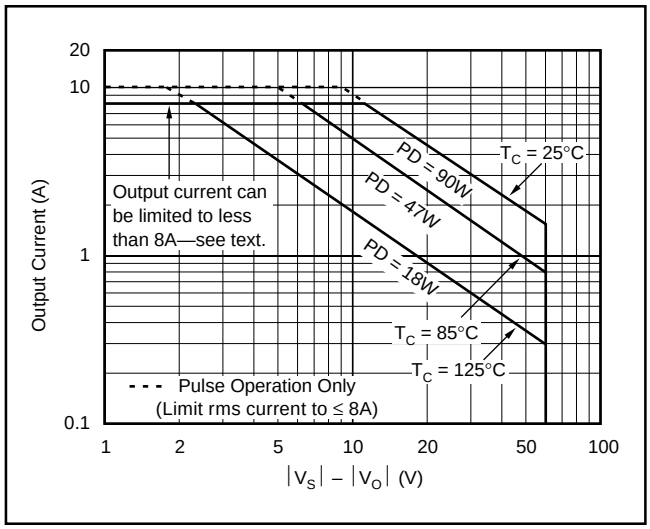


FIGURE 6. Safe Operating Area.

The safe output current decreases as $V_S - V_O$ increases. Output short circuits are a very demanding case for SOA. A short circuit to ground forces the full power-supply voltage (V+ or V–) across the conducting transistor. Increasing the case temperature reduces the safe output current that can be tolerated without activating the thermal shutdown circuit of the OPA549. For further insight on SOA, consult Application Report SBOA022 at the Texas Instruments web site (www.ti.com).

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower. Application Bulletin SBOA022 explains how to calculate or measure power dissipation with unusual signals and loads.

THERMAL PROTECTION

Power dissipated in the OPA549 will cause the junction temperature to rise. Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C and resets when the die has cooled to 140°C. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink) increase the ambient temperature until the thermal protection is triggered.

Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the OPA549 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the OPA549 into thermal shutdown will degrade reliability.

AMPLIFIER MOUNTING AND HEAT SINKING

Most applications require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the Equations:

$$T_J = T_A + P_D\theta_{JA} \quad (4)$$

where

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \quad (5)$$

T_J = Junction Temperature (°C)
T_A = Ambient Temperature (°C)
P_D = Power Dissipated (W)
θ_{JC} = Junction-to-Case Thermal Resistance (°C/W)
θ_{CH} = Case-to-Heat Sink Thermal Resistance (°C/W)
θ_{HA} = Heat Sink-to-Ambient Thermal Resistance (°C/W)
θ_{JA} = Junction-to-Air Thermal Resistance (°C/W)

Figure 7 shows maximum power dissipation versus ambient temperature with and without the use of a heat sink. Using a heat sink significantly increases the maximum power dissipation at a given ambient temperature, as shown in Figure 7.

The challenge in selecting the heat sink required lies in determining the power dissipated by the OPA549. For dc output, power dissipation is simply the load current times the voltage developed across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Other loads are not as simple. Consult the SBOA022 Application Report for further insight on calculating power dissipation. Once power dissipation for an application is known, the proper heat sink can be selected.

Heat Sink Selection Example—An 11-lead power ZIP package is dissipating 10 Watts. The maximum expected ambient temperature is 40°C. Find the proper heat sink to keep the junction temperature below 125°C (150°C minus 25°C safety margin).

Combining Equations (4) and (5) gives:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CH} + \theta_{HA}) \quad (6)$$

T_J, T_A, and P_D are given. θ_{JC} is provided in the Specifications Table, 1.4°C/W (dc). θ_{CH} can be obtained from the heat sink manufacturer. Its value depends on heat sink size, area, and material used. Semiconductor package type, mounting screw torque, insulating material used (if any), and thermal joint compound used (if any) also affect θ_{CH}. A typical θ_{CH} for a mounted 11-lead power ZIP package is 0.5°C/W. Now we can solve for θ_{HA}:

$\theta_{HA} = [(T_J - T_A)/P_D] - \theta_{JC} - \theta_{CH}$
$\theta_{HA} = [(125°C - 40°C)/10W] - 1.4°C/W - 0.5°C/W$
$\theta_{HA} = 6.6°C/W$

To maintain junction temperature below 125°C, the heat sink selected must have a θ_{HA} less than 6.6°C/W. In other words, the heat sink temperature rise above ambient must be less than 66°C (6.6°C/W • 10W). For example, at 10W Thermalloy model number 6396B has a heat sink temperature rise of 56°C (θ_{HA} = 56°C/10W = 5.6°C/W), which is below the required 66°C required in this example. Thermalloy model number 6399B has a sink temperature rise of 33°C (θ_{HA} = 33°C/10W = 3.3°C/W), which is also below the required 66°C required in this example. Figure 7 shows power dissipation versus ambient temperature for a 11-lead power ZIP package with the Thermalloy 6396B and 6399B heat sinks.

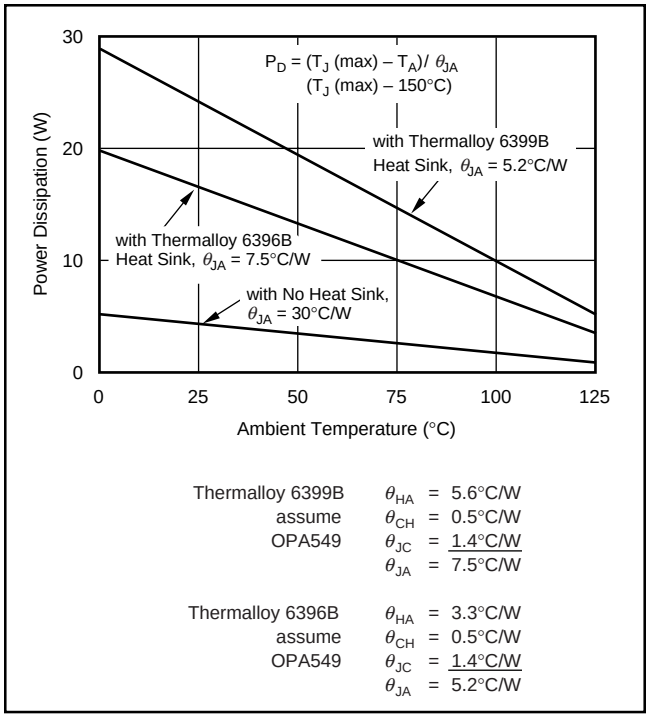


FIGURE 7. Maximum Power Dissipation vs Ambient Temperature.

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower θ_{CA} (θ_{CH} + θ_{HA}) dramatically. Some heat sink manufacturers provide thermal data for both of these cases. Heat sink performance is generally specified under idealized conditions that may be difficult to achieve in an actual application. For additional information on determining heat sink requirements, consult Application Report SBOA021.

As mentioned earlier, once a heat sink has been selected, the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection. Any tendency to activate the thermal protection circuitry may indicate inadequate heat sinking.

The tab of the 11-lead power ZIP package is electrically connected to the negative supply, V–. It may be desirable to isolate the tab of the 11-lead power ZIP package from its mounting surface with a mica (or other film) insulator. For lowest overall thermal resistance, it is best to isolate the entire heat sink/OPA549 structure from the mounting surface rather than to use an insulator between the semiconductor and heat sink.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. For normal operation, output compensation circuitry is typically not required. However, for difficult loads or if the OPA549 is intended to be driven into current limit, an R/C network may be required. Figure 8 shows an output R/C compensation (snubber) network which generally provides excellent stability.

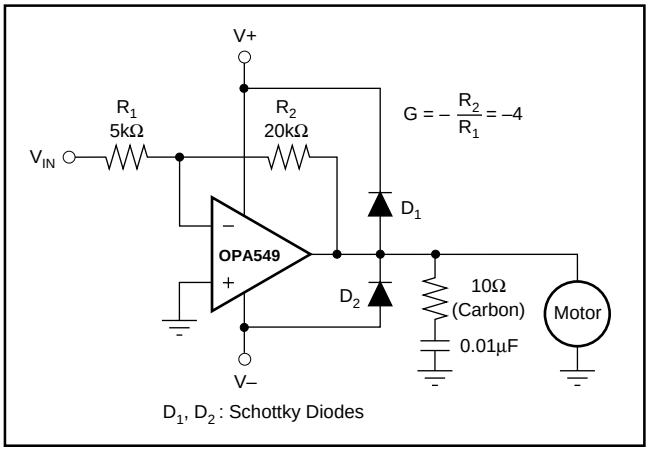


FIGURE 8. Motor Drive Circuit.

A snubber circuit may also enhance stability when driving large capacitive loads (> 1000pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically, 3Ω to 10Ω resistors in series with 0.01µF to 0.1µF capacitors is adequate. Some variations in circuit values may be required with certain loads.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 8. Schottky rectifier diodes with a 8A or greater continuous rating are recommended.

VOLTAGE SOURCE APPLICATION

Figure 9 illustrates how to use the OPA549 to provide an accurate voltage source with only three external resistors. First, the current limit resistor, R_{CL}, is chosen according to the desired output current. The resulting voltage at the I_{LIM} pin is constant and stable over temperature. This voltage, V_{CL}, is connected to the noninverting input of the op amp and used as a voltage reference, thus eliminating the need for an external reference. The feedback resistors are selected to gain V_{CL} to the desired output voltage level.

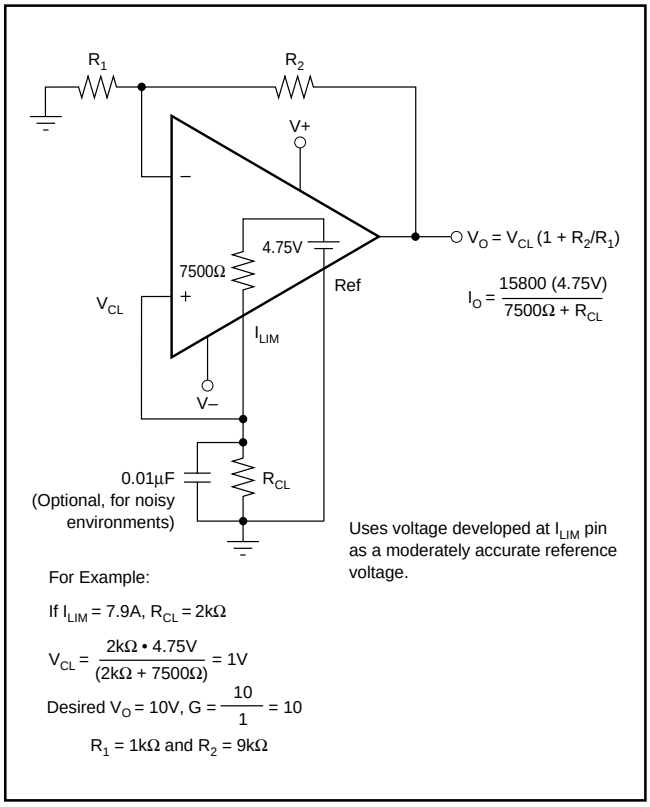


FIGURE 9. Voltage Source.

PROGRAMMABLE POWER SUPPLY

A programmable source/sink power supply can easily be built using the OPA549. Both the output voltage and output current are user-controlled. See Figure 10 for a circuit using potentiometers to adjust the output voltage and current while Figure 11 uses DACs. An LED connected to the E/S pin through a logic gate indicates if the OPA549 is in thermal shutdown.

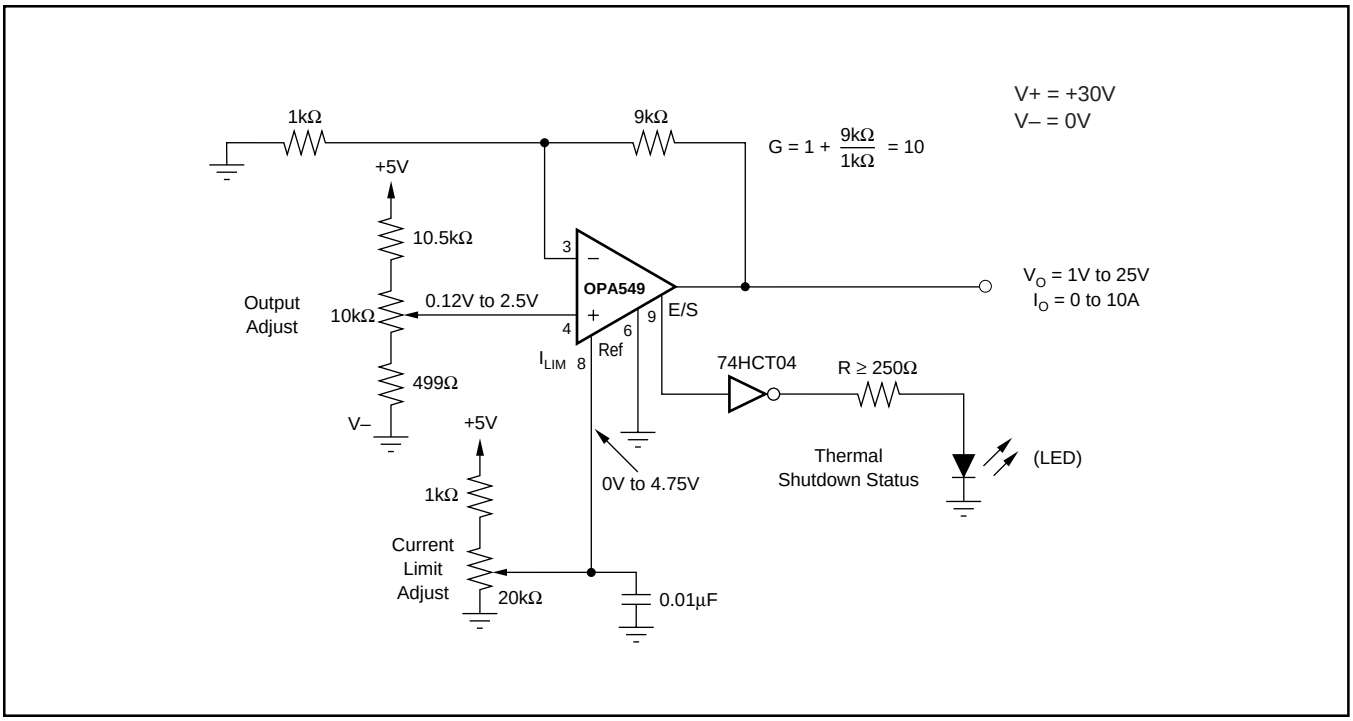


FIGURE 10. Resistor-Controlled Programmable Power Supply.

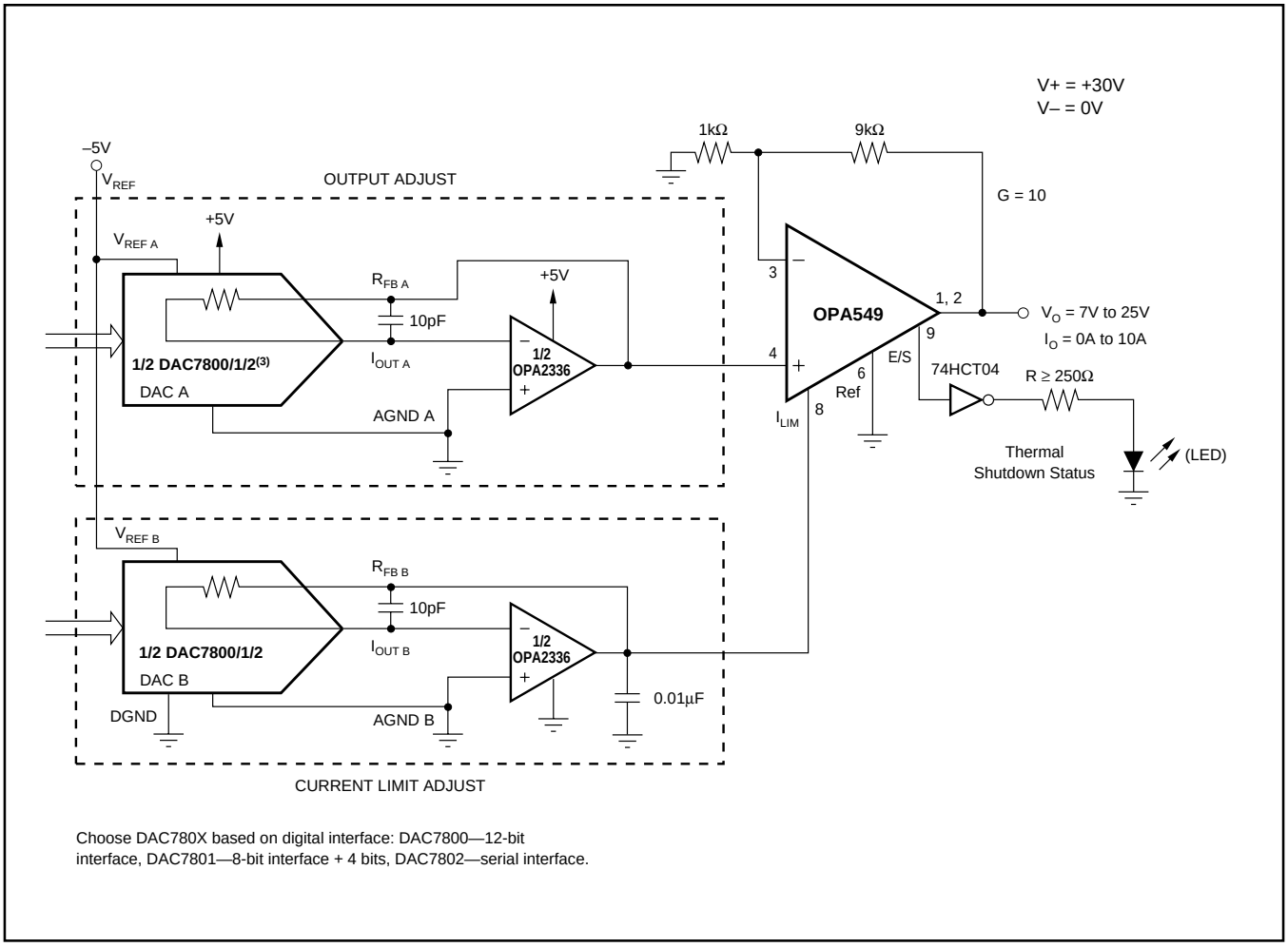


FIGURE 11. Digitally-Controlled Programmable Power Supply.

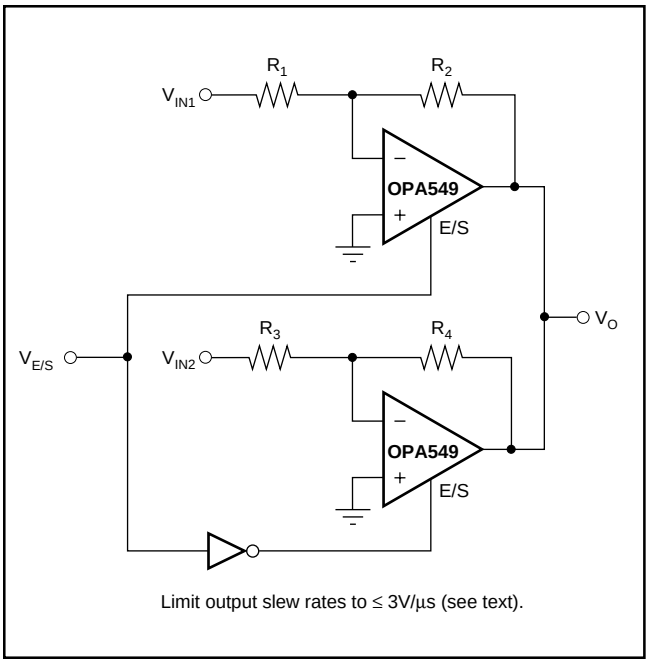


FIGURE 12. Switched Amplifier.

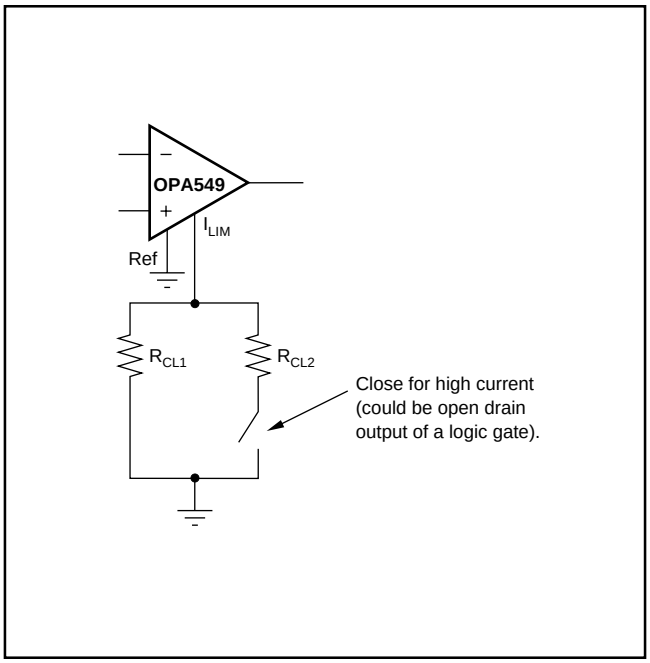


FIGURE 13. Multiple Current Limit Values.

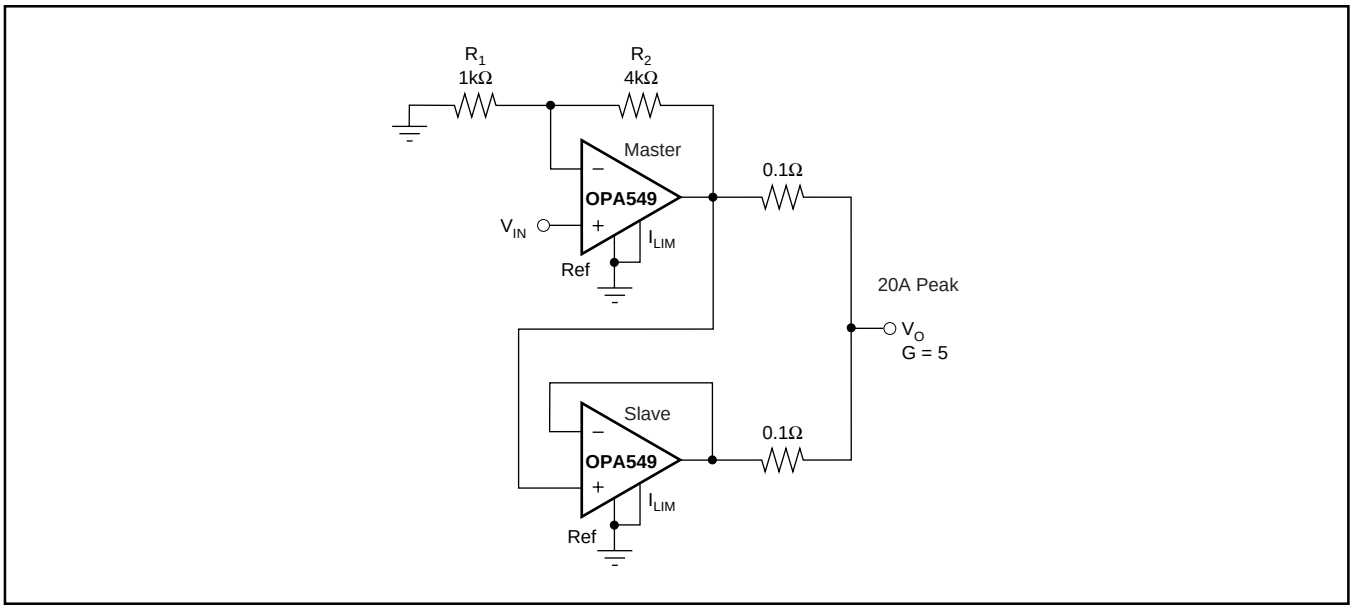


FIGURE 14. Parallel Output for Increased Output Current.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA549S	Active	Production	Power Package (KVC) | 11	25 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 85	OPA549S
OPA549S.A	Active	Production	Power Package (KVC) | 11	25 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 85	OPA549S
OPA549T	Active	Production	TO-220 (KV) | 11	25 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 85	OPA549T
OPA549T.A	Active	Production	TO-220 (KV) | 11	25 | TUBE	Yes	SN	N/A for Pkg Type	-40 to 85	OPA549T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

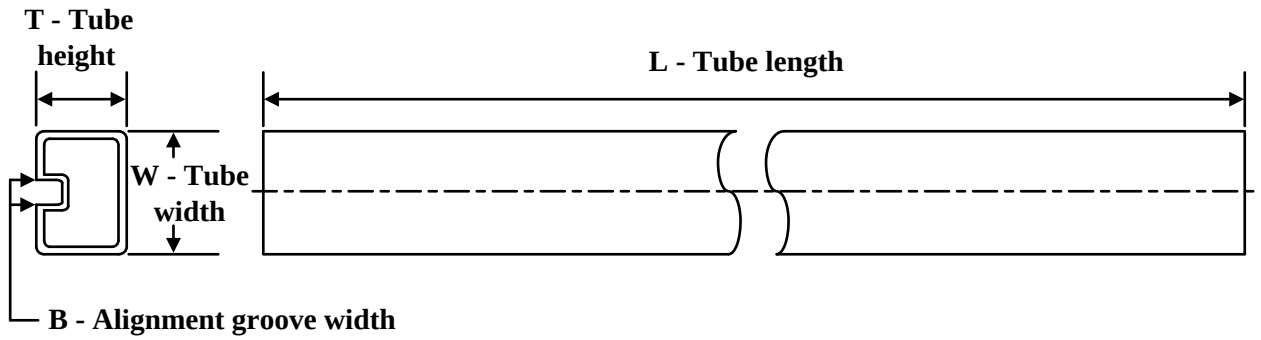
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

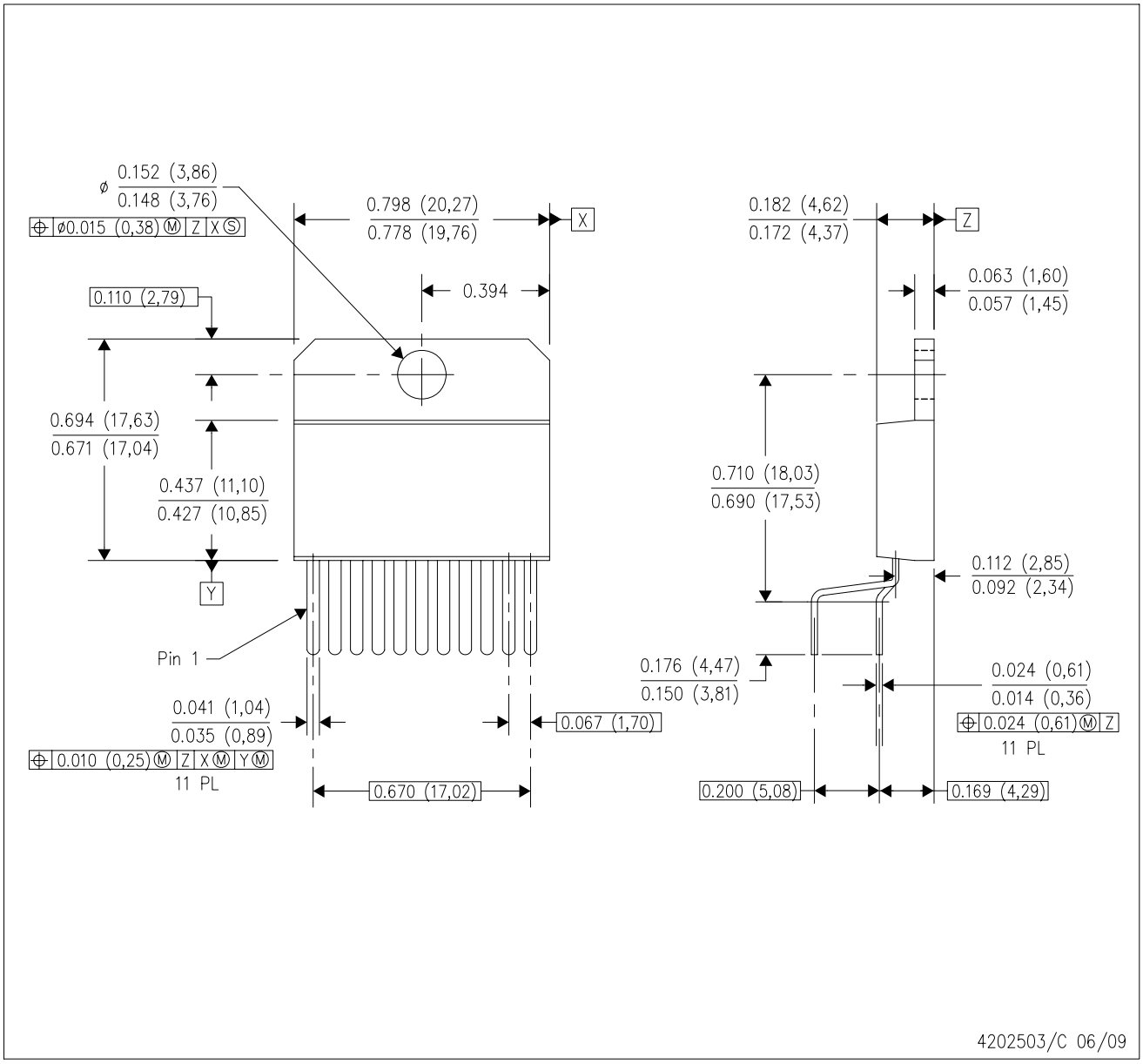
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA549S	KVC	TO-OTHER	11	25	532.13	36.32	13340	NA
OPA549S.A	KVC	TO-OTHER	11	25	532.13	36.32	13340	NA
OPA549T	KV	TO-220	11	25	532.13	36.32	13340	NA
OPA549T.A	KV	TO-220	11	25	532.13	36.32	13340	NA

KV (R–PZFM–T11) PLASTIC FLANGE–MOUNT



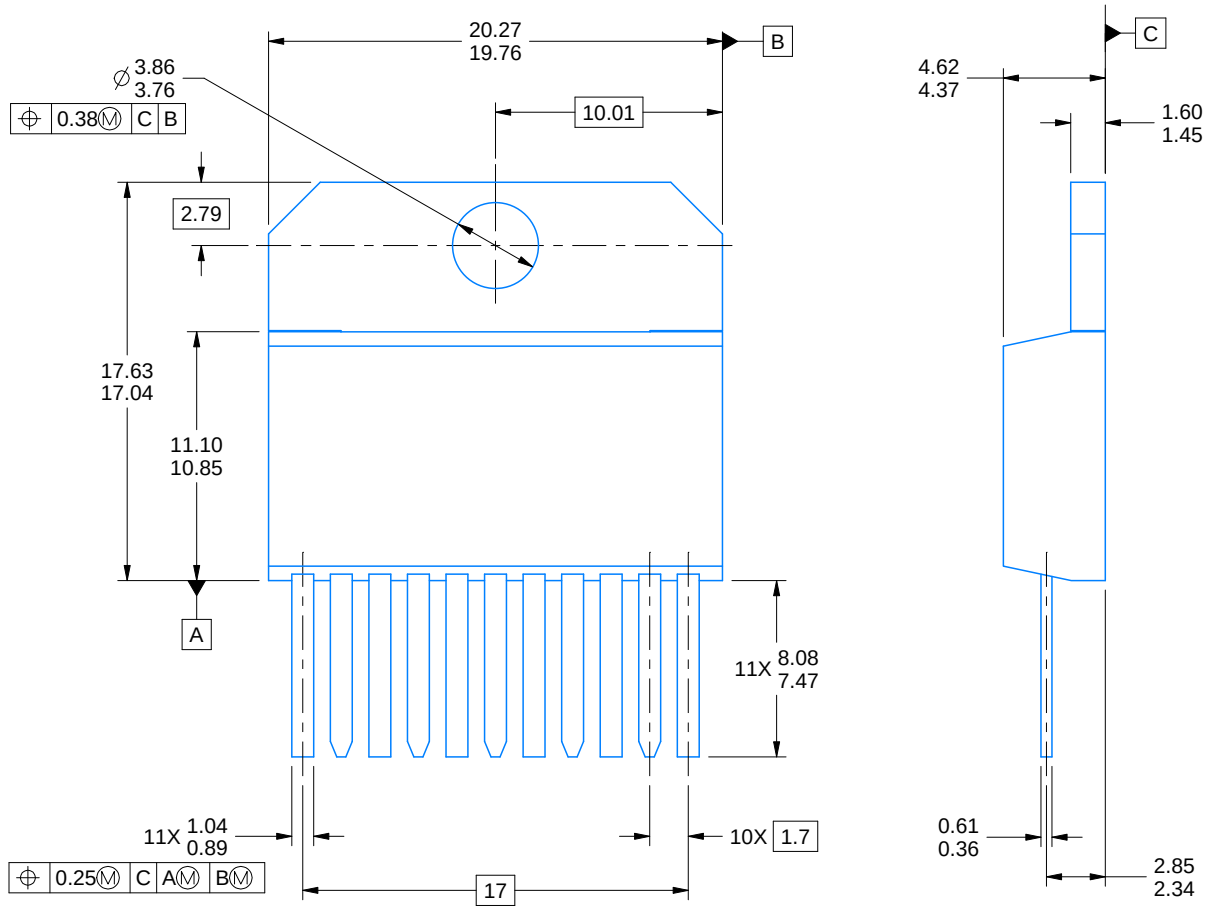
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension: inch.
D. All lead dimensions apply before solder dip.
E. Falls within JEDEC MO–48–AA.

PACKAGE OUTLINE

KVC0011A

TO - 4.62 mm max height

TRANSISTOR OUTLINE



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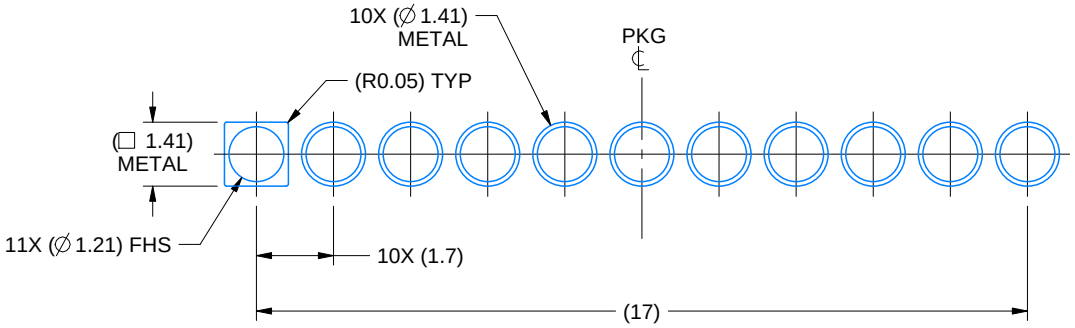
NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-48-AA. Reference for body dimensions only (excluding lead forming dimensions).



LAND PATTERN EXAMPLE
SCALE: 6X

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NOTES: (continued)

4. Refer to IPC-7251 which may have alternate design recommendations.

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