User's Guide

LP877451Q1EVM Evaluation Module

ABSTRACT

The LP87745-Q1 device is designed to meet the power management requirements of the AWR and IWR MMICs in various automotive and industrial radar applications. The device has three step-down DC/DC converters, a 5 V boost converter and a 1.8 V/3.3 V LDO. The LDO is powered from the boost and intended for xWR and peripheral devices IO supply. The device is controlled by an SPI serial interface and by enable signal. The step-down DC/DC converters support programmable switching frequency of 17.6 MHz, 8.8 MHz or 4.4 MHz and have low noise across wide frequency range which enables LDO-free power solution with minimal or no additional passive filtering. LP87745-Q1 device offers flexible external component selection to optimize the solution in terms of performance or cost. The features of the device target safety-relevant applications with system-safety requirements up to ASIL-C level.

This user's guide provides instructions to power up and evaluate LP87745-Q1 device using the LP877451Q1EVM evaluation module (EVM) and software user interface (LP87745-Q1 GUI). By default LP877451Q1EVM has LP877451A1RXVRQ1 device OTP version (17.6 MHz, Low noise use case BOM), but this EVM can also be used to evaluate another OTP device from LP8774x-Q1 product family.

CAUTION
Hot surface.
Contact may cause burns.
Do not touch!

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1 Top View with Basic External Connections

Figure 1-1 shows the top-view diagram of the EVM along with basic connections. By default, EVM is configured to power up through VBAT supply through onboard 12 V VIN to 3.3 V VOUT pre-regulator. EVM can also be powered through external 3.3 V supply or through USB port. Please refer to Table 3-2 for the right jumper configuration for each power-supply input.

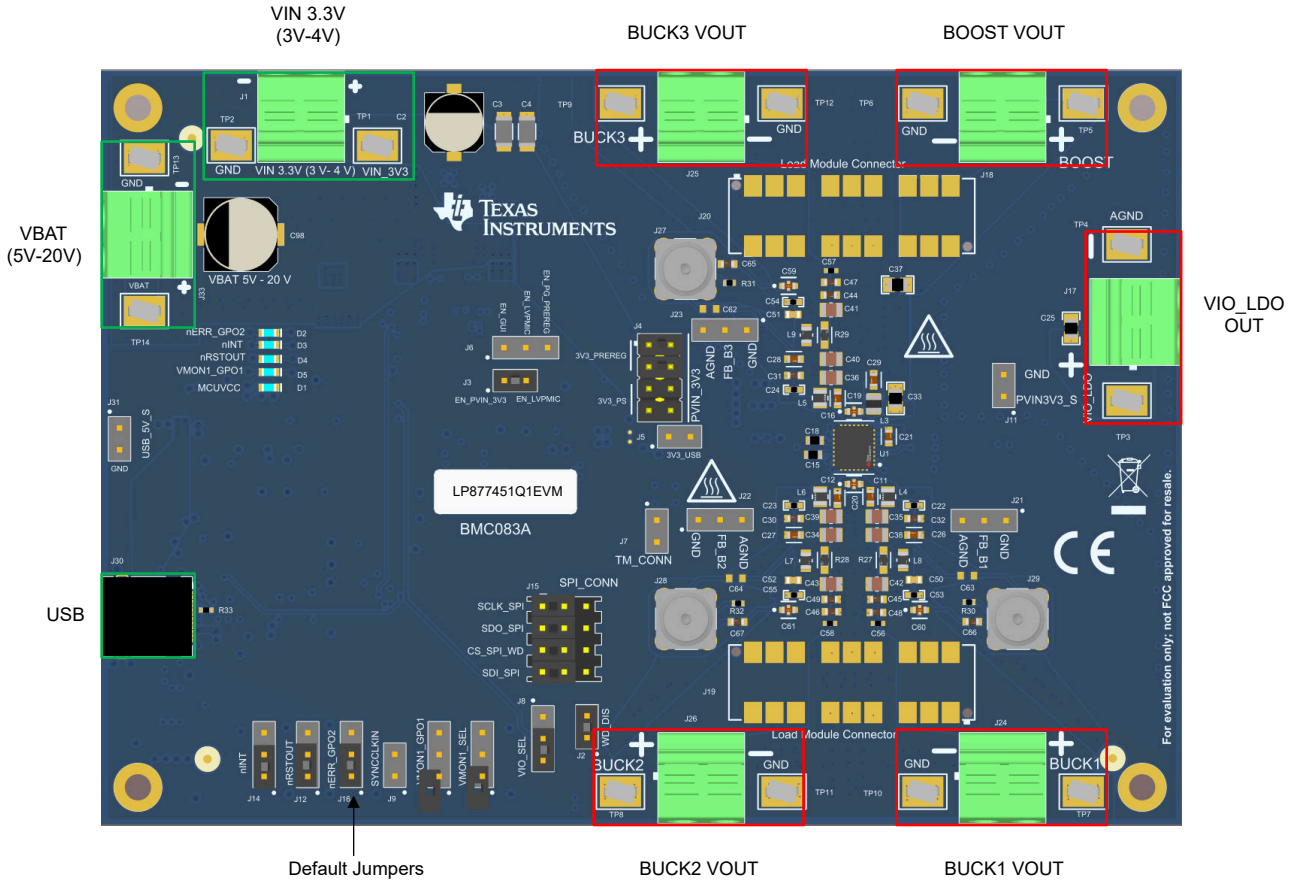

Figure 1-1. EVM Top-View Diagram With Basic Connections and Default Jumpers

2 Input, Output Voltages, and Load Current Requirements

LP87745-Q1 device works with 3.3 V input supply and supply is internally monitored for undervoltage (UV) and overvoltage (OV) conditions and hence keep the input supply voltage within 3.3 V +/- 8 % to avoid input supply UV/OV detection. Input power plane to the PMIC has option for additional filtering using L1 and L2 on the bottom side of the PCB.

- If the VBAT/preregulator path is used (default configuration), input supply to the device is already regulated to 3.3 V.
- If external 3.3 V supply is used, ensure that input supply voltage is always within the recommended voltage range and drop across supply path must be considered.
- If EVM is configured to work with USB supply, regulators should not be loaded.

Table 2-1 lists the input and output voltage for each regulator and their maximum load-current requirements. Refer LP87745-Q1 device data sheet for more information about device electrical characteristics and its features.

Table 2-1. Input and Output Voltages, and Load Current Requirements

Regulator Name	Input Supply Voltage at PMIC Supply Pin	Output Voltage	Maximum Load Current
BUCK1	3.04 V - 3.56 V	1.8 V	3 A
BUCK2	3.04 V - 3.56 V	1.0 V	3 A
BUCK3	3.04 V - 3.56 V	1.2 V	3 A
BOOST	3.04 V - 3.56 V	5 V	0.3 A
VIO_LDO	5 V (Generated from BOOST)	3.3 V	0.150 A

If all the regulators are loaded with maximum load current simultaneously, PMIC and PCB can become hot. Make sure that PMIC junction temperature does not exceed 150 °C.

3 Jumpers and connectors

LP877451Q1EVM has many terminal blocks, jumpers and test points to offer certain flexibility to help users to verify the EVM according to their application conditions. However, the EVM is pre-configured with default jumper settings and users can power up the regulators without the need of jumper modifications. Setting these jumpers correctly for the correct function of the EVM is important. Table 3-1 lists all the terminal blocks on the EVM and Table 3-2 lists the jumpers and their functionality. All the terminal blocks are marked with polarity and Pin 1 of test points / jumpers are marked with white dot for identification purpose. To understand more about the jumper functionality, see the schematic diagrams in Section 6.1.

Table 3-1. Terminal Blocks

Terminal Block Number	Terminal Block Name	Description
J1	VIN 3.3V	3.3 V External Input Voltage
J17	VIO_LDO	Terminal block for VIO_LDO Output
J18	BOOST	Terminal block for BOOST Output
J24	BUCK1	Terminal block for BUCK1 Output
J25	BUCK3	Terminal block for BUCK3 Output
J26	BUCK2	Terminal block for BUCK2 Output
J30	J30	USB Connector
J33	VBAT	5 V - 20 V Input

Table 3-2. Configuration Jumpers

Jumper/Connector Number	Jumper/Connector Name	Configuration	Description
J2	WD_DIS	Closed (Default)	Pull down resistor in CS_SPI pin enabled which will disable Q&A watchdog during the PMIC power up. For this to be effective, USB cable should not be connected to the EVM when the PMIC is powered up. If USB cable is connected before PMIC is powered up, USB MCU will drive this pin high (through CS_SPI_WD at J15) during the startup
		Open	Q&A watchdog not disabled during the PMIC power up
J3	EN_PVIN_3V3	Closed (Default)	Connects PMIC ENABLE pin to PVIN_Bx pins (PVIN_3V3) through a pull up resistor and device gets enabled as soon as 3.3 V is generated/applied
		Open	If PMIC needs to be enabled through USB/GUI or through pre-regulator PGOOD signal, then this jumper must be kept open
J4	PVIN_3V3	Option 1: Pins 1/3 and 2/4 3V3_PREREG (Default)	PVIN_3V3 connected to preregulator output. J4-Option-2 must be open and J5 must be open.
		Option 2: Pins 5/7 and 6/8 3V3_PS	PVIN_3V3 connected to external 3.3V supply (J1). J4-Option-1 must be open and J5 must be open.

Table 3-2. Configuration Jumpers (continued)

Jumper/Connector Number	Jumper/Connector Name	Configuration	Description
J5	3V3_USB	Open (Default)	Either option from J4 must be used.
		Closed	PMIC input supply (PVIN_3V3) is generated from USB supply. J4 jumpers must be open if this jumper is closed.
J6	EN_LVPMIC	Option 1: Open (Default)	PMIC Enable signal from 3.3 V Input. J3 must be closed
		Option 2: Pins 1 and 2	PMIC Enable signal path from GUI interface. J3 must be open if this Option is used
		Option 3: Pins 2 and 3	PMIC Enable signal path from pre-regulator PGOOD signal. J3 must be open if this Option is used
J8	VIO_SEL	Pins 1 and 2	3.3 V supply generated from USB supply
		Pins 2 and 3 (Default)	3.3 V VIO supply generated from PMIC VIO_LDO
J9	SYNCCLKIN	Pins 1 and 2	SYNCCLKIN pin connected to MCU clock port (used for testing external clock input signal)
J10	VMON1_SEL	Pins 1 and 2 (Default: open)	VMON1 reference voltage generated from voltage divider on VIO supply
		Pins 2 and 3 (Default: open)	VMON1 voltage taken from BUCK1 (1.8 V) output
J12	nRSTOUT	Pins 1 and 2 (Default)	Connects PMIC nRSTOUT signal to MCU port directly
		Pins 2 and 3	Connects PMIC nRSTOUT signal to MCU port through level shifter (series resistors must be mounted if this option is used)
J13	VMON1_GPO1	Pins 1 and 2 (Default: open)	Connects PMIC VMON1 signal to MCU port directly
		Pins 2 and 3 (Default: open)	Connects PMIC VMON1 signal to MCU port through level shifter (series resistors must be mounted if this option is used)
J14	nINT	Pins 1 and 2 (Default)	Connects PMIC nINT signal to MCU port directly
		Pins 2 and 3	Connects PMIC nINT signal to MCU port through level shifter (series resistors must be mounted if this option is used)

Table 3-2. Configuration Jumpers (continued)

Jumper/Connector Number	Jumper/Connector Name	Configuration	Description
J15	SCLK_SPI	Pins 1 and 2 (Default)	Connects PMIC SCLK_SPI signal to MCU SCLK_SPI port directly
		Pins 2 and 3	Connects PMIC SCLK_SPI signal to MCU SCLK_SPI port through a level shifter (series resistors need to be mounted if this option is used)
	SDO_SPI	Pins 1 and 2 (Default)	Connects PMIC SDO_SPI signal to MCU SDO_SPI port directly
		Pins 2 and 3	Connects PMIC SDO_SPI signal to MCU SDO_SPI port through a level shifter (series resistors need to be mounted if this option is used)
	CS_SPI_WD	Pins 1 and 2 (Default)	Connects PMIC CS_SPI signal to MCU CS_SPI port directly
		Pins 2 and 3	Connects PMIC CS_SPI signal to MCU CS_SPI port through a level shifter (series resistors must be mounted if this option is used)
	SDI_SPI	Pins 1 and 2 (Default)	Connects PMIC SDI_SPI signal to MCU SDI_SPI port directly
		Pins 2 and 3	Connects PMIC SDI_SPI signal to MCU SDI_SPI port through a level shifter (series resistors need to be mounted if this option is used)
J16	nERR_GPO2	Pins 1 and 2 (Default)	Connects PMIC nERR_GPO signal to MCU port directly
		Pins 2 and 3	Connects PMIC nERR_GPO2 signal to MCU port through level shifter (series resistors must be mounted if this option is used)

3.1 Test Points

Table 3-3 lists all the available connectors on the EVM.

Table 3-3. Test Points on the EVM

Connector Number	Connector Name	Description
J11	PVIN3V3_S	Test point to measure the input voltage of the PMIC
J19	Load Module Connector	Connector placeholder for PMICLOADBOARDEVM for doing load transient testing
J20	Load Module Connector	Connector placeholder for PMICLOADBOARDEVM for doing load transient testing
J21	FB_B1	Test point to measure the BUCK1 feedback signal
J22	FB_B2	Test point to measure the BUCK2 feedback signal
J23	FB_B3	Test point to measure the BUCK3 feedback signal
J27	J27	SMA connector for BUCK3 noise measurement
J28	J28	SMA connector for BUCK2 noise measurement

Table 3-3. Test Points on the EVM (continued)

Connector Number	Connector Name	Description
J29	J29	SMA connector for BUCK1 noise measurement
J31	USB_5V_S	Test point to measure 5 V supply from USB cable

4 Getting Started

In its default configuration, connecting +12 V and GND to the VBAT terminal block (J33) will power up the EVM. While loading the regulators, ensure that input power supply has sufficient current source capabilities to avoid supply voltage collapse due to current limiting.

EVM can also be powered through external 3.3 V input supply or through USB power by modifying jumper settings on the EVM. Table 4-1 describes the jumper settings for different supply options.

Table 4-1. Jumper Connections for Powering the EVM

Power Source	Input Voltage Range	Jumpers
VBAT	5 V - 20 V	Both 3V3_PREREG jumpers in J4 (Default option). Leave J5 open.
Vin 3.3V	3.1 V - 3.5 V	Remove 3V3_PREREG jumpers on J4 and place them on 3V3_PS position on J4. With this configuration, do not apply power to VBAT terminal. Leave J5 open.
USB	5 V USB cable	J5, 3V3_USB. With this option, jumpers on J4 must be removed.

The LP877451Q1EVM does not require any specific power-down sequence. The EVM can be powered down by turning off the power supply or by toggling the EN Pin off in the GUI, if the GUI control signal is used to enable/disable the device. Refer to Table 3-2 and GUI section for more information about configuring jumpers and using GUI.

4.1 GUI

Texas Instruments provides a simple to use LP87745-Q1 GUI tool to enable, configure, and evaluate the various features of the LP87745-Q1 device on the EVM. Please refer to the GUI *README.md* file in the GUI tool's *Help->View README.md* tab for a more detailed description of this tool.

The GUI will run on most PC platforms and requires a USB port for connecting the EVM to the host computer. The EVM USB connector is type-C and a type-A to type-C cable is provided along with the EVM to connect to the host computer. EVM will get automatically connected to the GUI after the USB cable is connected and manual assignment of COM port is not necessary. If *Hardware not Connected* displays on the bottom left of the GUI, clicking *Click to connect to hardware* icon next to it will re-establish the connection. The GUI uses the ACCtrl COM port which can be found from the device manager of the operating system.

4.2 GUI Installation and working with GUI

The GUI can be found here and it can be run in browser or it can be installed to the computer. Figure 4-1 shows the default interface of GUI. Please refer to the *README.md* file in the GUI tool for a complete guide on how to use the tool.

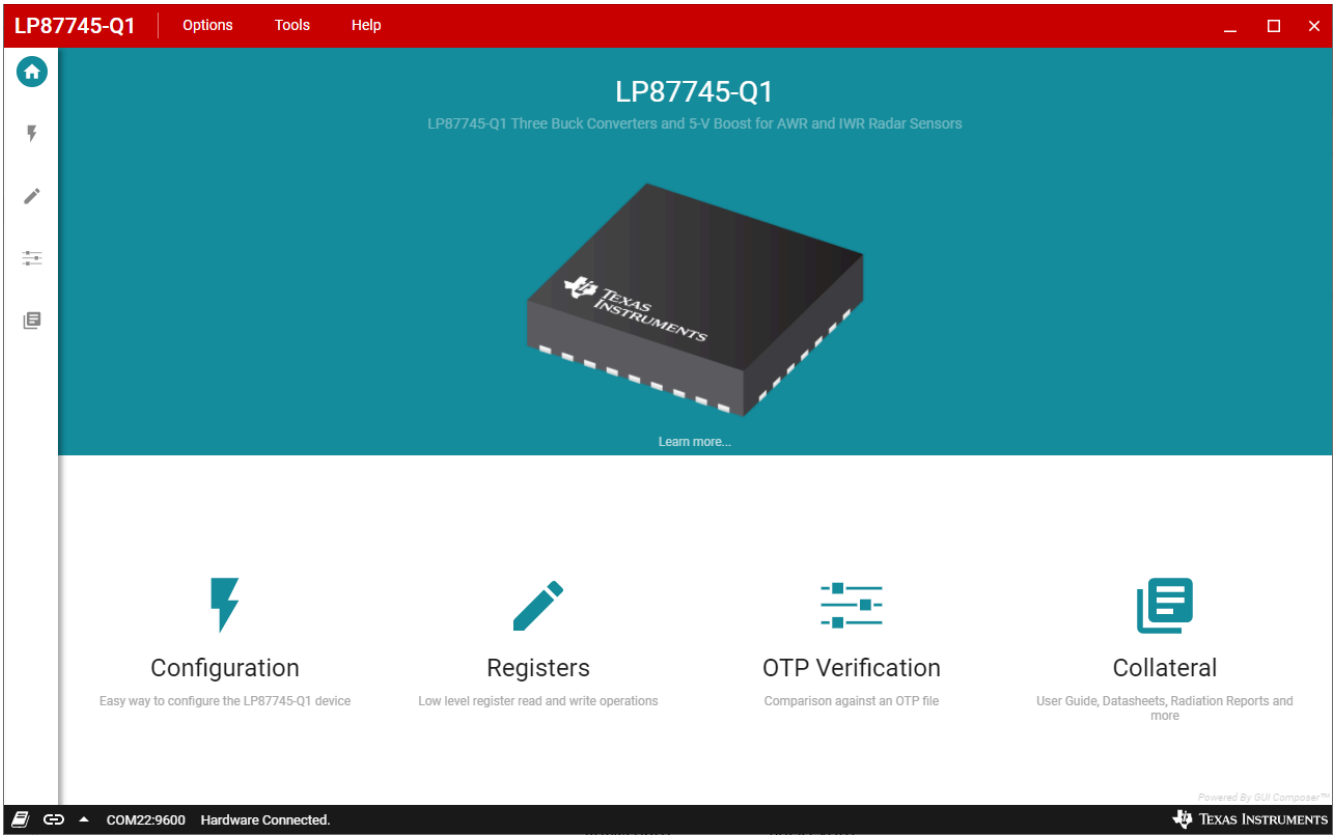

Figure 4-1. GUI Front Page

The EVM can be configured in the configuration page shown in Figure 4-2. By default, all the configuration registers are locked and CRC protected. Clicking the *Unlock registers* check box on the Configuration Page will automatically write REGISTER_LOCK_STATUS =0x9B to unlock the configuration registers for write operation. CRC can be disabled by writing CONFIG_CRC_EN = 0h through Console window (Options → Show Console) or GUI Register Map Page. For example, output voltages, startup and shutdown delays and peak current limits can be changed for each buck converter.

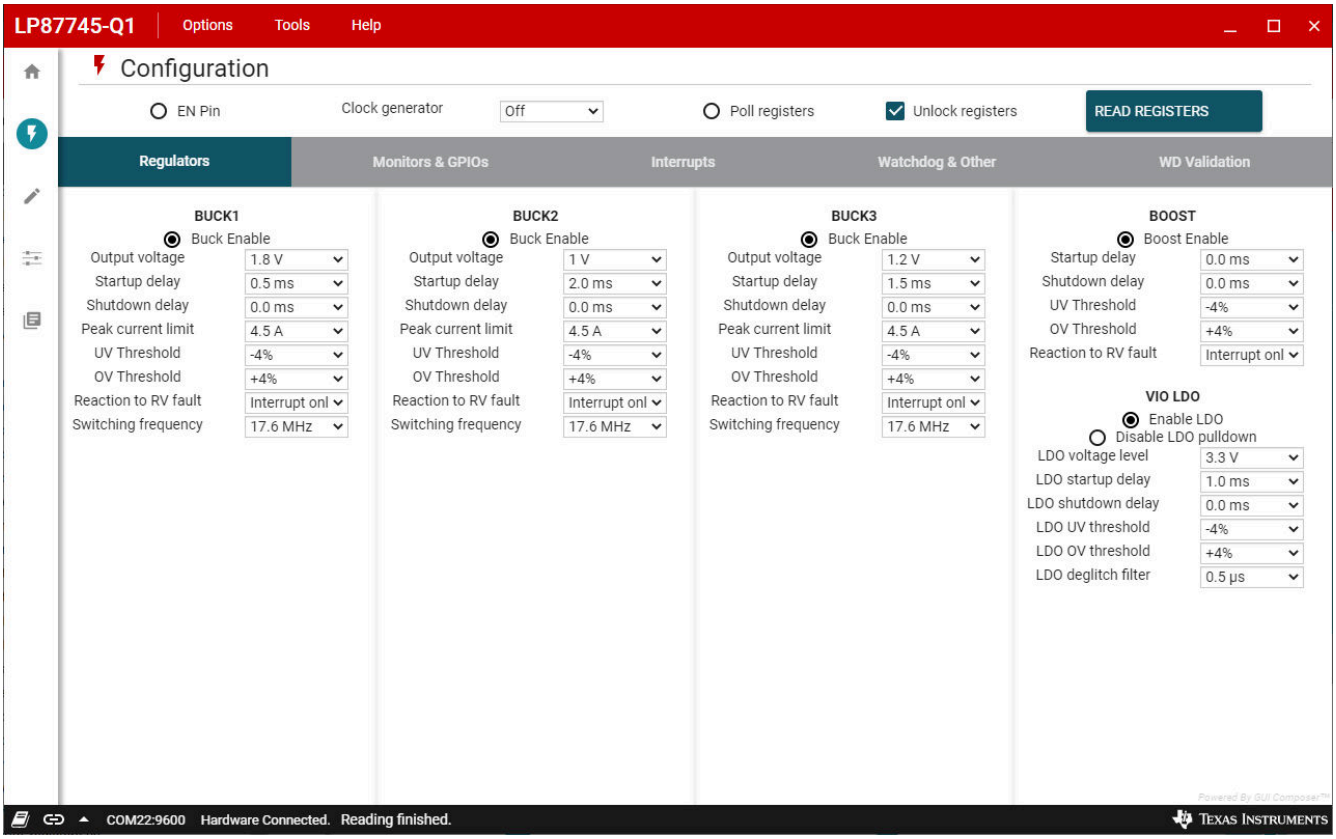

Figure 4-2. GUI Configuration Page

In the register map page shown in Figure 4-3, registers can be read or written to.

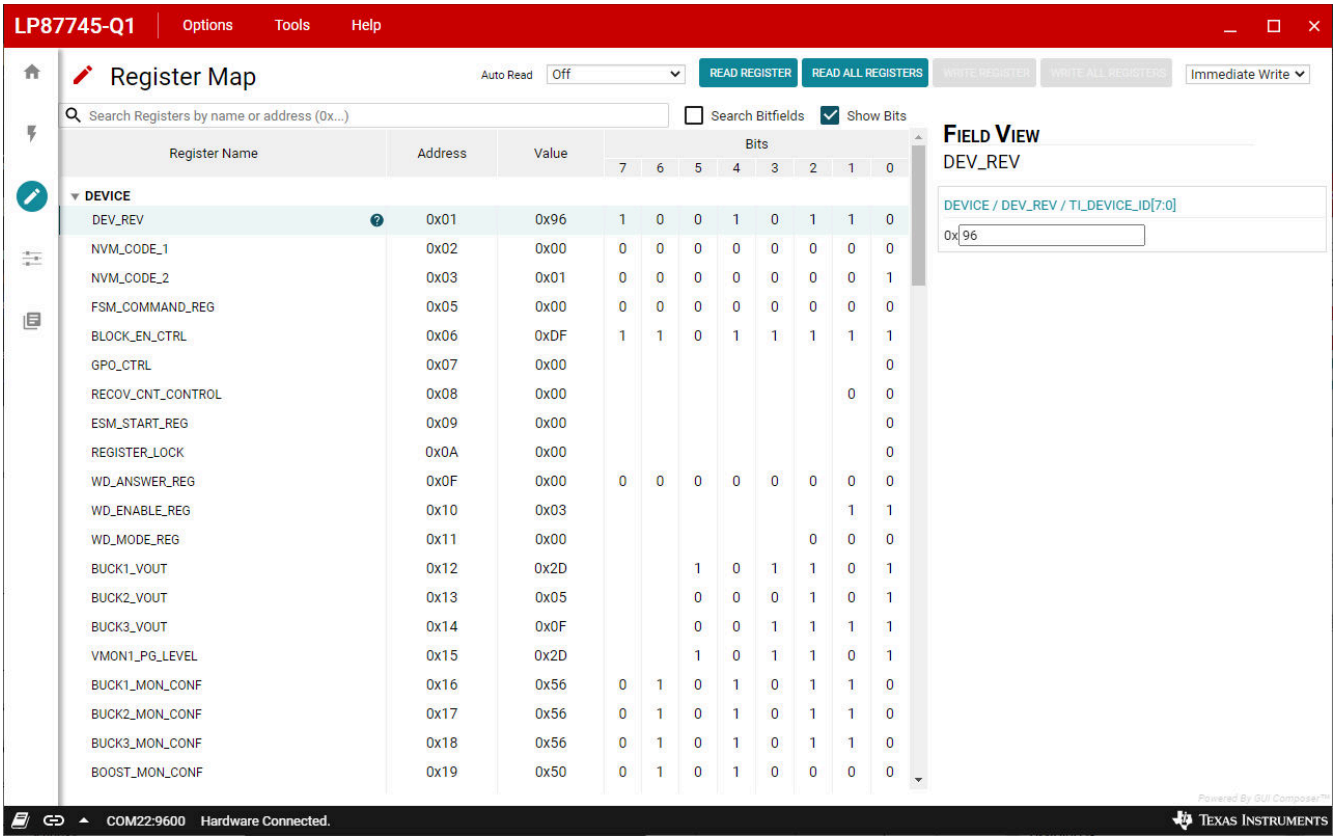

Figure 4-3. GUI Register Map Page

5 Watchdog

This section provides the basic overview of the SPI based Q&A watchdog algorithm implemented on the EVM. Please refer LP87745-Q1 device data sheet for more detailed information about device watchdog functionality. This watchdog requires specific SPI messages from the host MCU in specific time intervals to detect correct operation of the MCU. On the EVM, MSP432 MCU is used as a host MCU.

During operation, the device provides a 4-bit question for the MCU and the MCU calculates the required 32-bit answer. This answer is split into four answer bytes: Answer-3, Answer-2, Answer-1 and Answer-0. The MCU writes these answer bytes one byte at a time into WD_ANSWER[7:0] from the SPI interface.

A good event occurs when the MCU sends the correct answer-bytes calculated for the current question in the correct watchdog window and in the correct sequence. This sequence is visualized in Figure 5-1

A bad event occurs when one of the events that follows occur:

- The MCU sends the correct answer-bytes, but not in the correct watchdog window.
- The MCU sends incorrect answer-bytes.
- The MCU returns correct answer-bytes, but in the incorrect sequence.

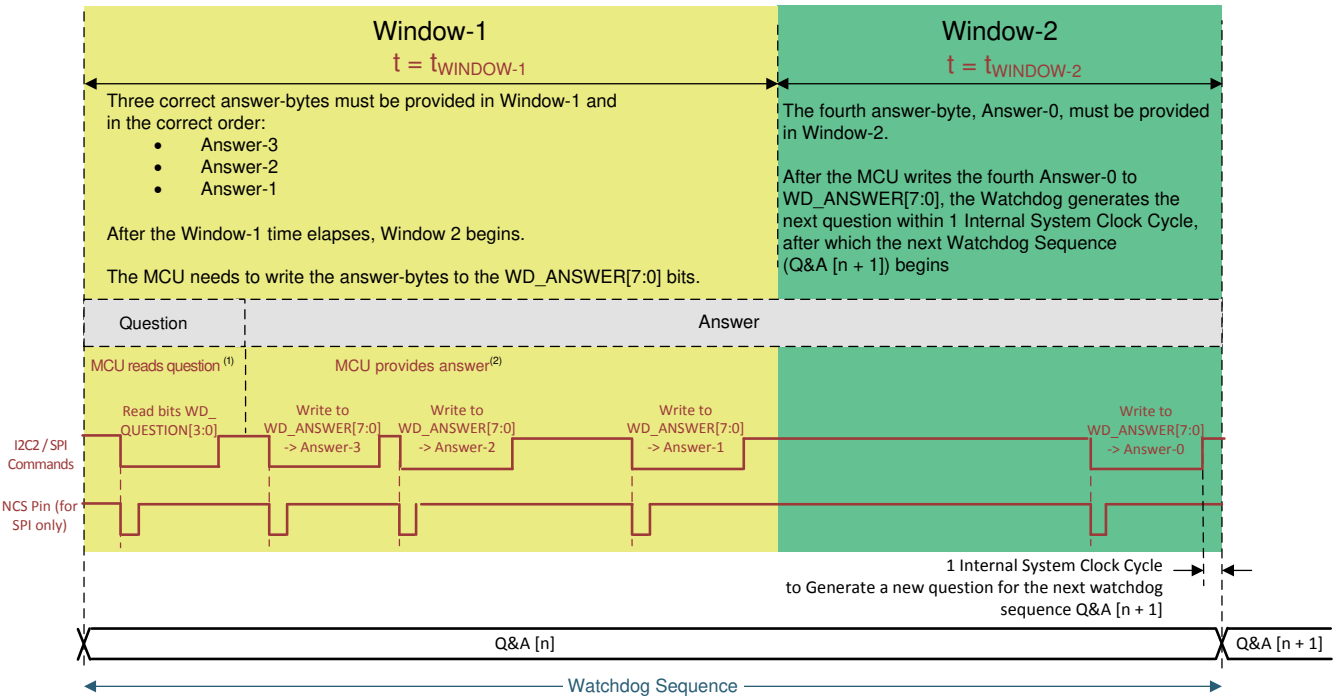

Figure 5-1. Watchdog Sequence in Q&A Mode

In GUI, there are two sections in configuration tab for watchdog configurability. Figure 5-2 illustrates the watchdog validation section in GUI, where the delays between the WD Answers can be configured and watchdog status for different interrupts and errors can be observed. And if required status can be cleared through clear buttons available next to the each status. In the other watchdog configuration section, watchdog can be enabled or disabled along with other watchdog configurable parameters as shown in Figure 5-3. For further information on watchdog configuration, refer to the data sheet of LP8774x-Q1 SNVSBE7 for watchdog section.

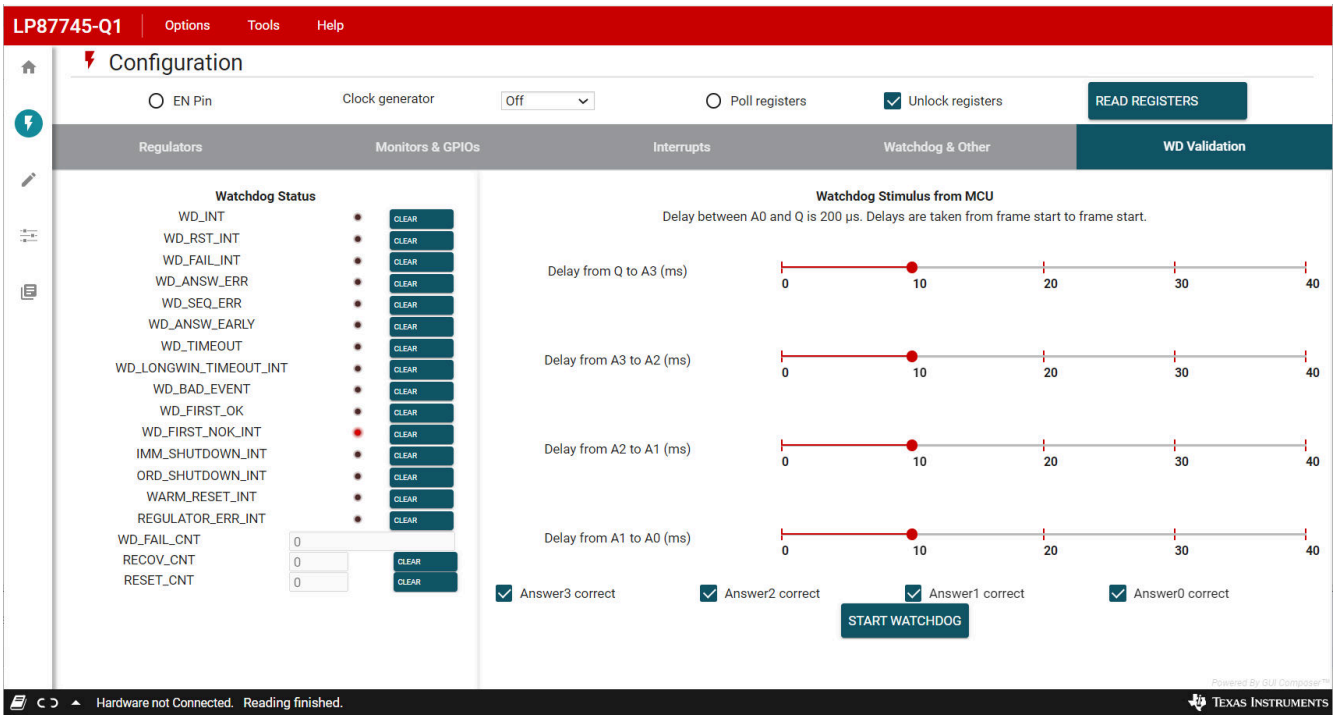

Figure 5-2. GUI Watchdog Validation Configuration

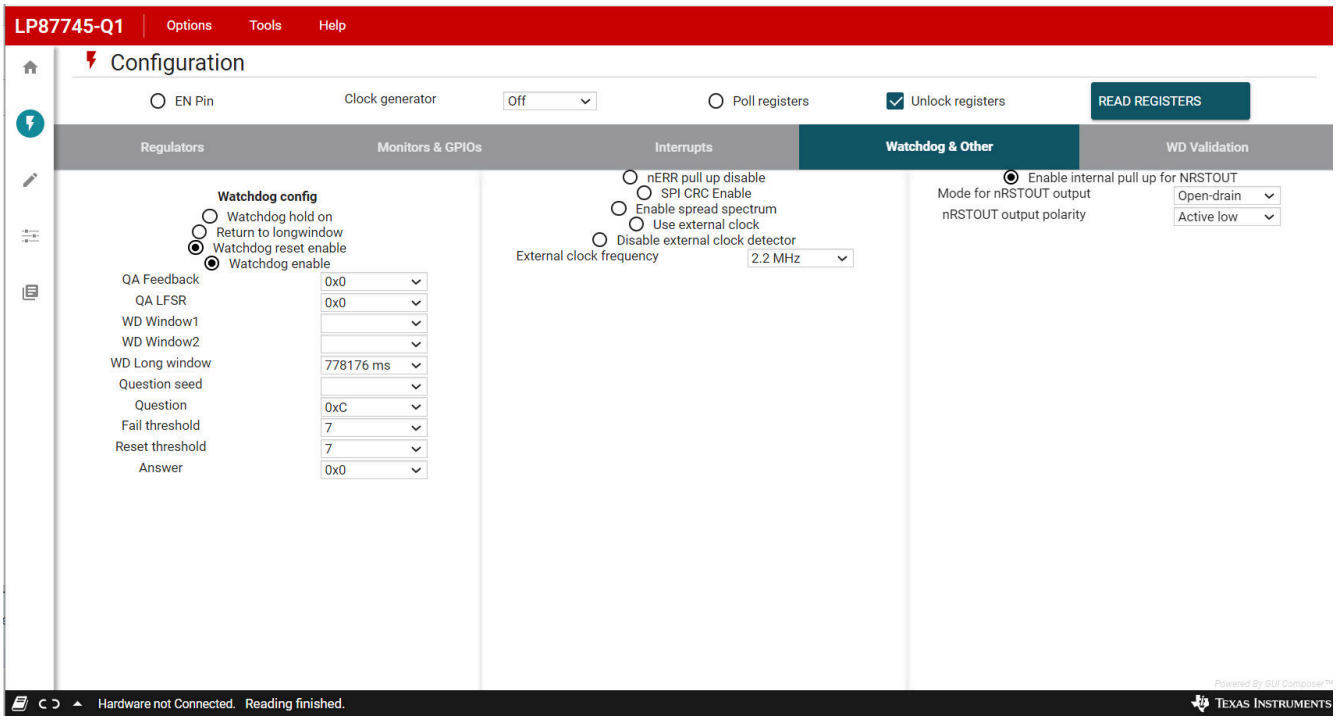

Figure 5-3. GUI Watchdog Configuration

6 Schematics, Layout and BOM

This section contains the schematics, layout and the bill of materials for the LP87745Q1EVM.

6.1 Schematic Diagram

This section includes images of the EVM schematics and different layers of the layout.

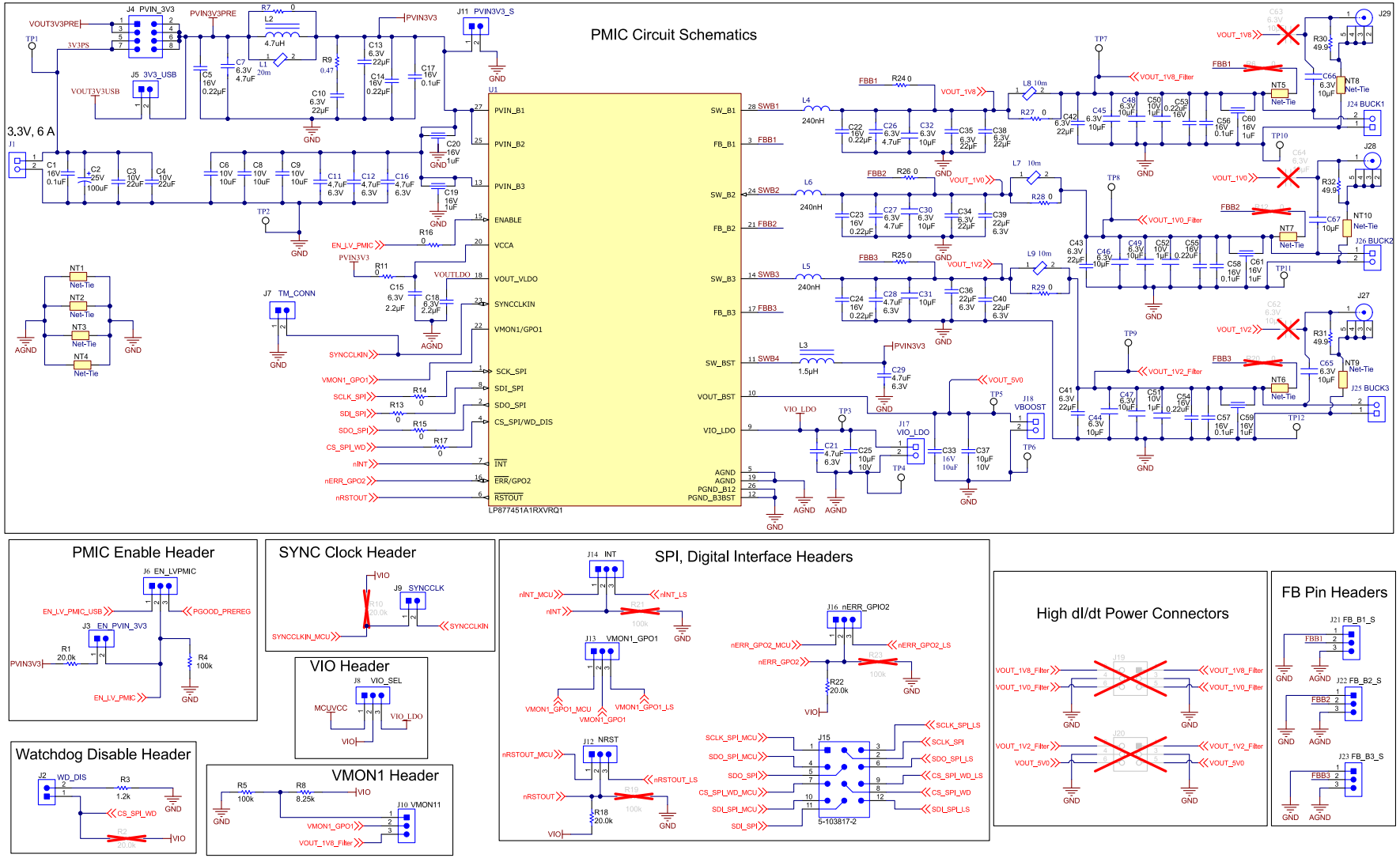

Figure 6-1. PMIC Schematic

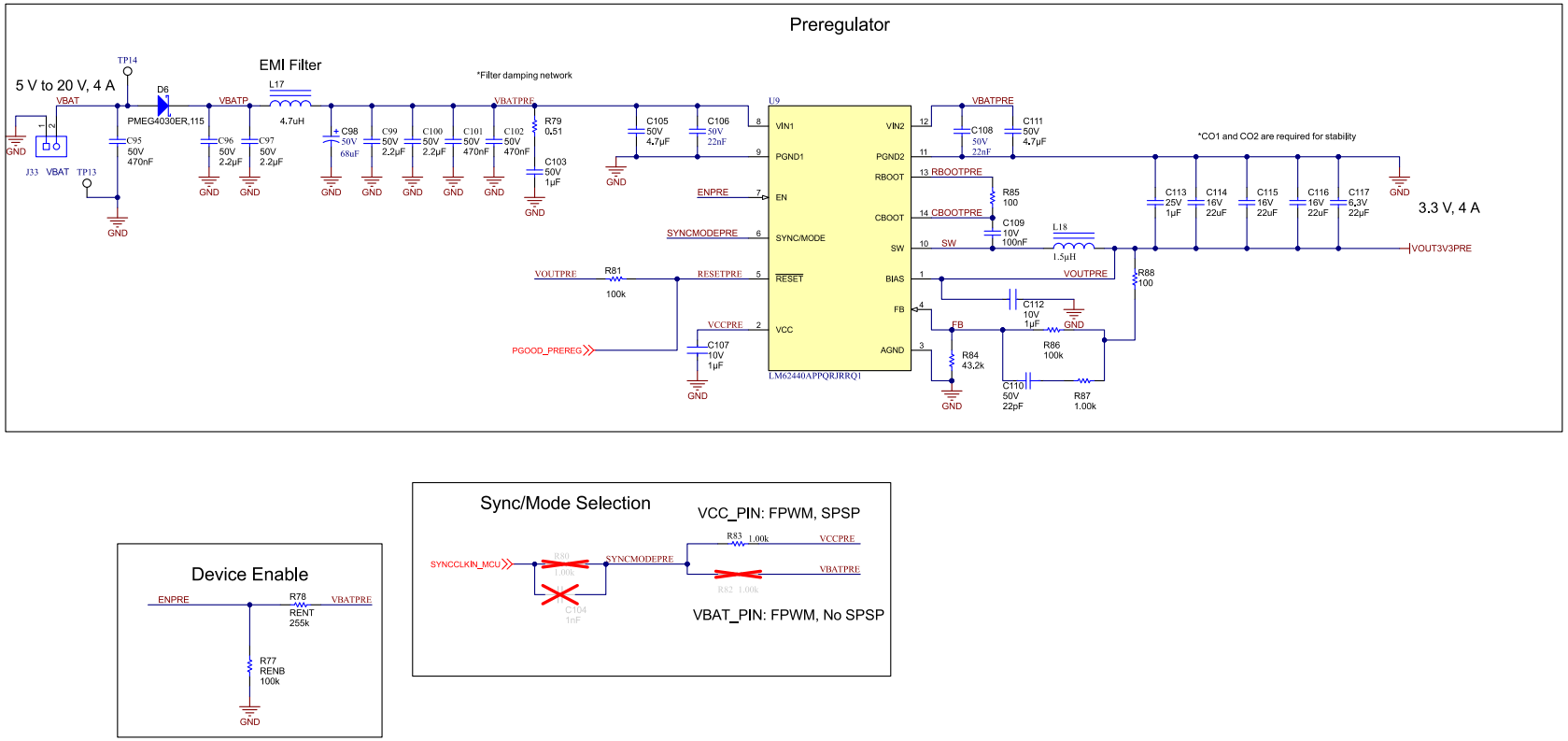

Figure 6-2. Preregulator Schematic

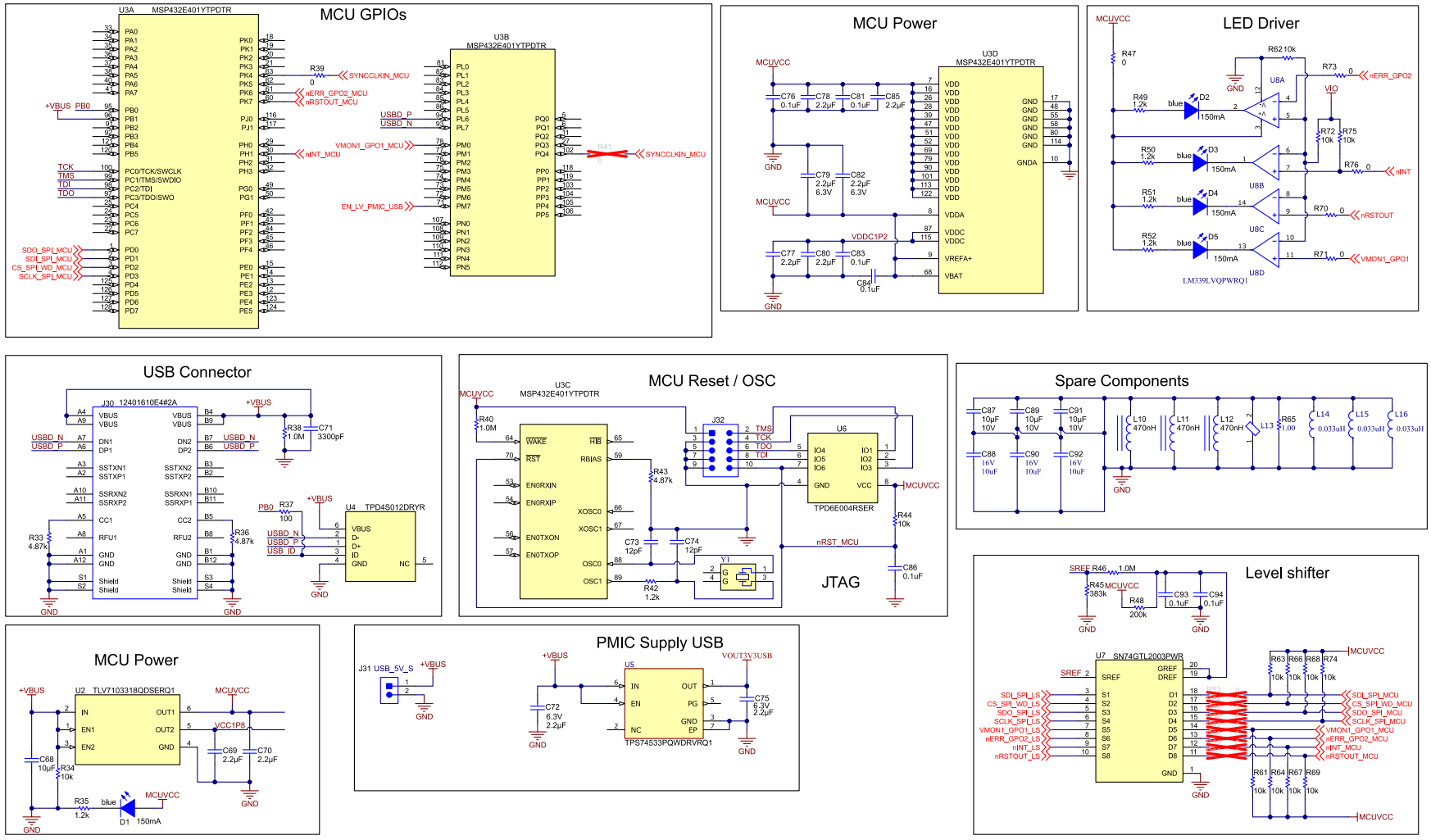

Figure 6-3. MCU Schematic

6.2 PCB Layer Diagram

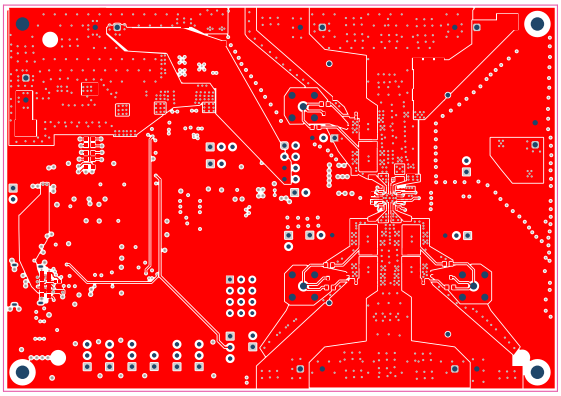

Figure 6-4. Layout of Top Layer, Layer 1

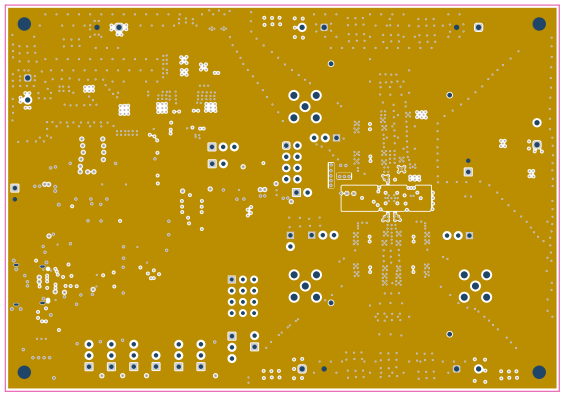

Figure 6-5. Layout of Ground layer 1, Layer 2

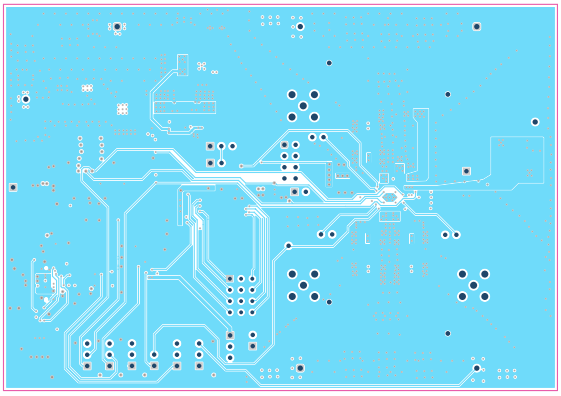

Figure 6-6. Layout of Signal Layer 1, Layer 3

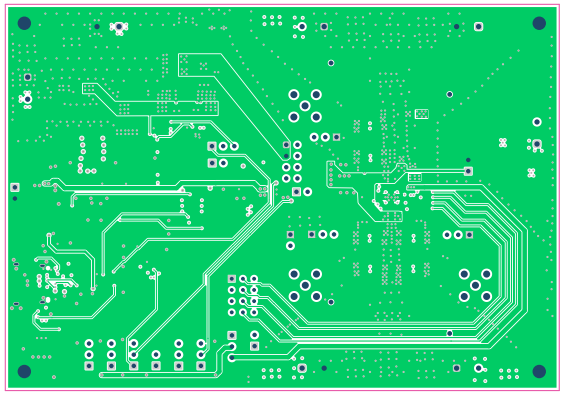

Figure 6-7. Layout of Signal Layer 2, Layer 4

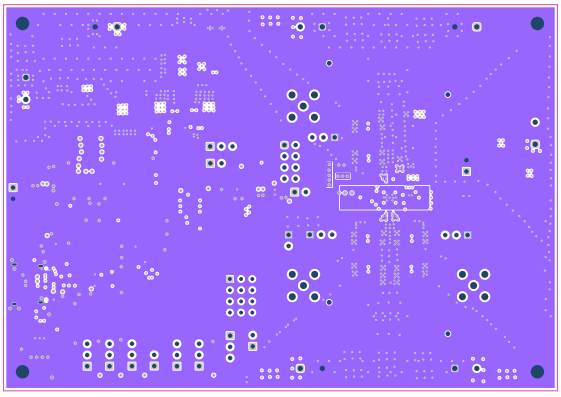

Figure 6-8. Layout of Ground Layer 2, Layer 5

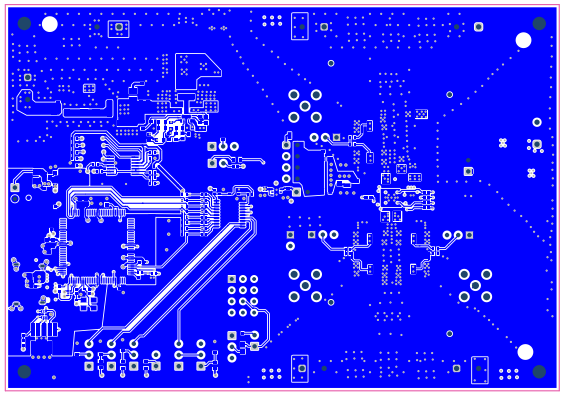

Figure 6-9. Layout of Bottom Layer, Layer 6

6.3 Components List

Table 6-1 lists all the components on the EVM.

Table 6-1. Components list

Designator	Quantity	Description	PartNumber	Manufacturer
!PCB1	1	Printed Circuit Board	BMC083	Any
C1, C17, C56, C57, C58, C76, C81, C83, C84, C86, C93, C94	12	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	GCM155R71C104KA55D	MuRata

Table 6-1. Components list (continued)

Designator	Quantity	Description	PartNumber	Manufacturer
C2	1	CAP, Polymer Hybrid, 100 uF, 25 V, +/- 20%, 30 ohm, 6.3x7.7 SMD	EEHZC1E101XP	Panasonic
C3, C4	2	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	GCM31CR71A226KE02L	MuRata
C5, C14, C22, C23, C24	5	CAP, CERM, 0.22 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	MuRata
C6, C8, C9, C25, C37, C68, C87, C89, C91	9	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	GCM21BR71A106KE22L	MuRata
C7, C11, C12, C16, C21, C26, C27, C28, C29	9	Cap Ceramic Multilayer 4.7uF 6.3V DC 10% SMD Paper T/R	GCJ188C70J475KE02J	Murata
C10, C13, C34, C35, C36, C38, C39, C40, C41, C42, C43, C117	12	CAP, CERM, 22 µF, 6.3 V,+/- 20%, X7T, AEC-Q200 Grade 1, 0805	CGA4J1X7T0J226M	TDK
C15, C18	2	CAP, CERM, 2.2 µF, 6.3 V,+/- 10%, X7R, 0603	GCM188R70J225KE22J	MuRata
C19, C20, C59, C60, C61	5	3 Terminals Low ESL Chip Multilayer Ceramic Capacitors for Automotive	NFM18HC105C1C3D	Murata
C30, C31, C32, C44, C45, C46, C47, C48, C49, C65, C66, C67	12	Chip Multilayer Ceramic Capacitors for Automotive	GCM188D70J106ME36D	Murata
C33, C88, C90, C92	4	CAP, CERM, 10 uF, 16 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	CGA4J1X7S1C106K125AC	TDK
C50, C51, C52, C107, C112	5	CAP CER 0603 1UF 10V X7R 10%	C0603C105K8RACAUTO	KEMET
C53, C54, C55	3	CAP, CERM, 0.22 uF, 16 V, +/- 10%, X7R, 0402	GRM155R71C224KA12D	MuRata
C69, C70, C72, C75, C77, C78, C79, C80, C82, C85	10	CAP, CERM, 2.2 uF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	MuRata
C71	1	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0603	C0603C332K5RACTU	Kemet
C73, C74	2	CAP, CERM, 12 pF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H120J050BA	TDK
C95, C101, C102	3	CAP, CERM, 0.47 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E3X7R1H474K080AE	TDK
C96, C97, C99, C100	4	CAP, CERM, 2.2 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	CGA4J3X7R1H225K125AB	TDK
C98	1	CAP, Polymer Hybrid, 68 uF, 50 V, +/- 20%, 30 ohm, 8x10 SMD	EEHZA1H680P	Panasonic
C103	1	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	UMK107AB7105KA-T	Taiyo Yuden
C105, C111	2	CAP, CERM, 4.7 µF, 50 V,+/- 20%, X7R, AEC-Q200 Grade 1, 1210	UMK325B7475MMHT	Taiyo Yuden
C106, C108	2	CAP, CERM, 0.022 uF, 50 V, +/- 10%, X7R, 0402	GRM155R71H223KA12D	MuRata
C109	1	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	C0603X104K8RACTU	Kemet
C110	1	C0603 22 pF X7R 30ppm/°C 10.00% 50 V	C0603C220K5RACAUTO	KEMET
C113	1	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0805	C0805C105K3RACTU	Kemet

Table 6-1. Components list (continued)

Designator	Quantity	Description	PartNumber	Manufacturer
C114, C115, C116	3	CAP, CERM, 22 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	CGA6P1X7R1C226M250AC	TDK
D1, D2, D3, D4, D5	5	LED, Blue, SMD	LB Q39G-L2N2-35-1	OSRAM
D6	1	Diode, Schottky, 40 V, 3 A, AEC-Q101, SOD-123W	PMEG4030ER,115	Nexperia
H1, H4, H5, H7	4		FC2058-440-A	Fascomp
H2, H3, H6, H8	4	MACHINE SCREW PAN PHILLIPS 4-40	9900	Keystone
J1, J17, J18, J24, J25, J26, J33	7	Terminal Block, 5mm, 2x1, R/A, TH	1792863	Phoenix Contact
J2, J3, J5, J7, J9, J11, J31	7	Header, 100mil, 2x1, Gold, TH	HTSW-102-07-G-S	Samtec
J4	1	Header, 2.54mm, 4x2, Gold, TH	TSW-104-08-L-D	Samtec
J6, J8, J10, J12, J13, J14, J16, J21, J22, J23	10	Header, 100mil, 3x1, Gold, TH	HTSW-103-07-G-S	Samtec
J15	1	Header, 2.54mm, 4x3, Gold, TH	5-103817-2	TE Connectivity
J27, J28, J29	3	SMA Jack, Straight, 50 Ohm, Gold, TH	SMA-J-P-H-ST-TH1	Samtec
J30	1	Receptacle, 0.5mm, USB TYPE C, R/A, SMT	12401610E4#2A	Amphenol Canada
J32	1	Header (Shrouded), 1.27mm, 5x2, Gold, SMT	FTSH-105-01-F-DV-K	Samtec
L1	1	100 Ohms @ 100MHz 1 Power Line Ferrite Bead 0805 (2012 Metric) 4A 20mOhm	MPZ2012S101ATD25	TDK
L2, L17	2	Inductor, Shielded, Composite, 4.7 uH, 4.5 A, 0.0401 ohm, SMD	XAL4030-472MEB	Coilcraft
L3	1	Inductor, Shielded, Metal Composite, 1.5 µH, 2.3 A, 0.11 ohm, AEC-Q200 Grade 0, SMD	TFM201610ALMA1R5MTAA	TDK
L4, L5, L6	3	240nH Shielded Thin Film Inductor 5A 23mOhm Max 0806 (2016 Metric)	TFM201610ALMAR24MTAA	TDK
L7, L8, L9, L13	4	30 Ohms @ 100MHz 1 Power Line Ferrite Bead 0805 (2012 Metric) 6A 10mOhm	MPZ2012S300ATD25	TDK
L10, L11, L12	3	Inductor, Shielded, Metal Composite, 470 nH, 3.9 A, 0.039 ohm, AEC-Q200 Grade 0, SMD	TFM201610ALMAR47MTAA	TDK
L14, L15, L16	3	Fixed Inductor 0.033uH 30% 4.7A 9mOhm 0603	TFM160810ALTA33NNTAA	TDK
L18	1	Inductor, Shielded, Metal Composite, 1.5 µH, 5.8 A, 0.019 ohm, SMD	74438356015	Wurth Elektronik
LBL1	1		THT-14-423-10	Brady
R1, R18, R22	3	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K0FKEA	Vishay-Dale
R3, R35, R42, R49, R50, R51, R52	7	RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021K20JNED	Vishay-Dale
R4, R5, R77, R81, R86	5	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
R7, R27, R28, R29	4	RES 0 OHM JUMPER 1/4W 0603	HCJ0603ZT0R00	Stackpole Electronics
R8	1	RES, 8.25 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06038K25FKEA	Vishay-Dale

Table 6-1. Components list (continued)

Designator	Quantity	Description	PartNumber	Manufacturer
R9	1	RES, 0.47, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3RQFR47V	Panasonic
R11	1	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0EDHP	Vishay-Dale
R13, R14, R15, R16, R17, R47, R70, R71, R73, R76	10	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0ED	Vishay-Dale
R24, R25, R26, R39	4	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GE0R00X	Panasonic
R30, R31, R32	3	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	RMCF0402FT49R9	Stackpole Electronics Inc
R33, R36, R43	3	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04024K87FKED	Vishay-Dale
R34, R44, R61, R62, R63, R64, R66, R67, R68, R69, R72, R74, R75	13	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040210K0JNED	Vishay-Dale
R37	1	RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402100RJNED	Vishay-Dale
R38, R40, R46	3	RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021M00JNED	Vishay-Dale
R45	1	RES, 383 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402383KFKED	Vishay-Dale
R48	1	RES, 200 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402200KJNED	Vishay-Dale
R65	1	RES, 1.00, 1%, 0.1 W, 0603	RC0603FR-071RL	Yageo
R78	1	RES, 255 k, 1%, 0.1 W, 0603	RC0603FR-07255KL	Yageo
R79	1	RES, 0.51, 1%, 0.25 W, 0805	CRM0805-FX-R510ELF	Bourns
R83	1	RES, 1.00 k, 1%, 0.1 W, 0603	RC0603FR-071KL	Yageo
R84	1	RES, 43.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060343K2FKEA	Vishay-Dale
R85	1	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100RJNEA	Vishay-Dale
R87	1	RES, 1.00 k, 1%, 0.1 W, 0603	ERJ-3EKF1001V	Panasonic
R88	1	RES, 100, 1%, 0.1 W, 0603	RC0603FR-07100RL	Yageo
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14	14	Shunt, 100mil, Gold plated, Black	881545-2	TE Connectivity
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14	14	Test Point, Compact, SMT	5016	Keystone
U1	1	Three Buck Converters and 5-V Boost for AWR and IWR Radar Sensors	LP877451A1RXVRQ1	Texas Instruments
U2	1	Automotive Catalog, Dual, 200mA, Low-IQ Low-Dropout Regulator for Portable Devices, DSE0006A (WSON-6)	TLV7103318QDSERQ1	Texas Instruments

Table 6-1. Components list (continued)

Designator	Quantity	Description	PartNumber	Manufacturer
U3	1	MSP432E401YTPDT, PDT0128A (TQFP-128)	MSP432E401YTPDTR	Texas Instruments
U4	1	4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6)	TPD4S012DRYR	Texas Instruments
U5	1	Linear Voltage Regulator IC 1 Output 500mA 6-WSON (2x2)	TPS74533PQWDRVRQ1	Texas Instruments
U6	1	Low-Capacitance 6-Channel +/-15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8)	TPD6E004RSER	Texas Instruments
U7	1	8-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR, PW0020A (TSSOP-20)	SN74GTL2003PWR	Texas Instruments
U8	1	Automotive 5.5-V low-voltage standard quad-channel comparator with 1-microsecond delay 14-TSSOP -40 to 125	LM339LVQPWRQ1	Texas Instruments
U9	1	Automotive 4 A Low Noise Synchronous Buck Regulators, RJR0014A (VQFN-HR-14)	LM62440APPQRJRRQ1	Texas Instruments
Y1	1	Crystal, 25 MHz, 20 ppm, AEC-Q200 Grade 1, SMD	ECS-250-12-33Q-JES-TR	ECS Inc.
C62, C63, C64	0	Chip Multilayer Ceramic Capacitors for Automotive	GCM188D70J106ME36D	Murata
C104	0	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	C0603C102K5RACTU	Kemet
J19, J20	0	Receptacle, 2.5mm, 3x2, Gold, SMT	6651712-1	TE Connectivity
R2, R10	0	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K0FKEA	Vishay-Dale
R6, R12, R20, R53, R54, R55, R56, R57, R58, R59, R60	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0ED	Vishay-Dale
R19, R21, R23	0	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
R41	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GE0R00X	Panasonic
R80, R82	0	RES, 1.00 k, 1%, 0.1 W, 0603	RC0603FR-071KL	Yageo

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2021) to Revision A (October 2022) **Page**

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