Technical White Paper

Understanding Functional Safety FIT Base Failure Rate Estimates per IEC 62380 and SN 29500

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ABSTRACT

Functional safety standards like International Electrotechnical Commission (IEC) 61508 [1] and International Organization for Standardization (ISO) 26262 [2] require that semiconductor device manufacturers address both systematic and random hardware failures. Systematic failures are managed and mitigated by following rigorous development processes. Random hardware failures must adhere to specified quantitative metrics to meet hardware safety integrity levels (SILs) or automotive SILs (ASILs). Consequently, systematic failures are excluded from the calculation of random hardware failure metrics.

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Trademarks

1 Introduction

Base failure rates (BFR) quantify the intrinsic reliability of the semiconductor component while operating under *normal* environmental conditions. BFR is typically multiplied by factors such as temperature, voltage and number of operating hours to arrive at a quantitative measure of the *quality* of the component.

One of the primary inputs for calculating random hardware metrics (as required by functional safety standards) is the BFR. It can be estimated by a variety of techniques. BFR estimation techniques rely on assumptions of failure modes; thus, differences in these underlying assumptions lead to differences in BFR estimations.

This paper focuses on two widely accepted techniques to estimate the BFR for semiconductor components; estimates per IEC Technical Report 62380 [3] and SN 29500 [4] respectively. BFR estimation is foundational to calculate quantitative random hardware metrics, including: and IEC

- Safe failure fraction (SFF)
- Probability of failure per hour (PFH) in high-demand mode; or probability of failure per day (PFD) in low demand mode
- Single-point fault metric (SPFM)
- Latent fault metric (LFM)
- Probabilistic metric for random hardware failure (PMHF)

This paper also outlines factors that influence BFR and compares and contrasts the various techniques.

2 Types of Faults and Quantitative Random Hardware Failure Metrics

Hardware faults can be either systematic or random in nature, as shown in Figure 2-1. Systematic faults result from an inadequacy in the design, development or manufacturing process and typically stem from gaps in the development process. A silicon bug is a systematic fault because it is detectable during the design verification phase of development. For example, designing a car and specifying that it has square wheels is considered a systematic fault because the car does not work with that shape of wheel. By adhering to a rigorous development process, it is possible to manage and mitigate systematic faults – and even eliminate them completely – by making continuous process improvements.

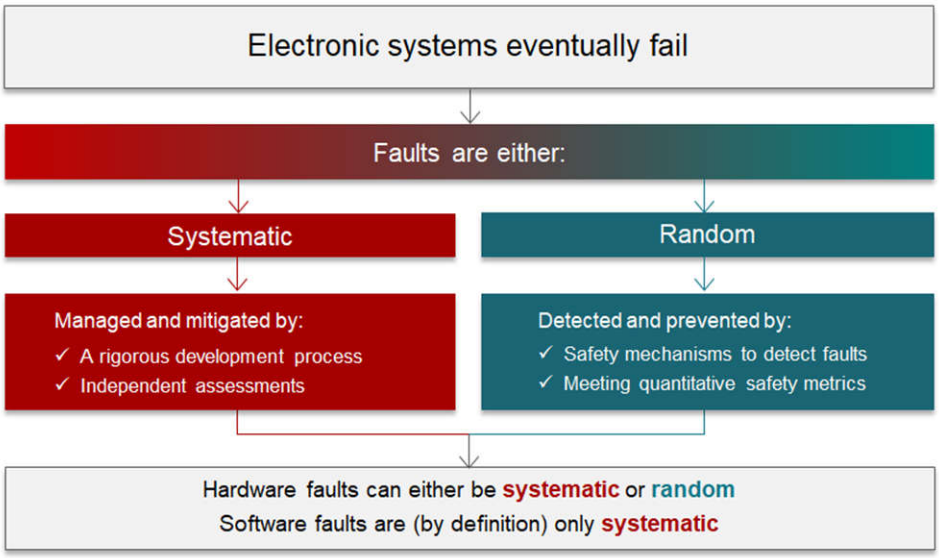


Figure 2-1. Overview of Systematic and Random Faults

Conversely, random hardware faults cannot be eliminated. These faults arise from the fact that all electronic systems fail eventually. Consequently, the ability to address random hardware faults is limited to detecting and possibly preventing them. In the case of automotive electrical, electronic and programmable electronic systems, alerting drivers to a problem enables some control over the impact of random hardware faults.

Table 2-1 and Table 2-2 list the acceptable values of random hardware failure metrics associated with each ASIL or SIL value according to the requirements of ISO 26262 and IEC 61508 respectively.

Table 2-1. Hardware Failure Metrics According to ISO 26262-5

ASIL Level	SPFM	LFM	PMHF (in FIT; Failures in Time)
ASIL B	≥90%	≥60%	≤100 FIT
ASIL C	≥97%	≥80%	≤100 FIT
ASIL D	≥99%	≥90%	≤10 FIT

Table 2-2. Hardware Failure Metrics According to IEC 61508-3

SIL Level	SFF	PFH (in FIT; Failures in Time)
SIL 2	≥90%	≤1000 FIT
SIL 3	≥99%	≤10 FIT

Both IEC 61508 and ISO 26262 exclude systematic failures while calculating random hardware metrics. Consequently, BFR is only applicable to the failure mode distribution and calculation of random hardware metrics.

3 Random Failures Over a Product Lifetime and Estimation of BFR

Figure 3-1 shows the bathtub curve, a classic representation of random hardware faults over three key periods of a semiconductor product's lifetime. These are:

- **Early life failures (also known as infant mortality)**: characterized by a relatively higher *initial* failure rate, which reduces rapidly. It is possible to further minimize early life failures by performing accelerated life tests (like burn-in or I_{DDQ} testing) which are done as a part of Texas Instruments (TI) outgoing test in the factory. Early-life failures are primarily caused by manufacturing defects that are not effectively screened. Defects are unavoidable. Developing and continuously improving effective screening is a requirement.
- **Normal life failures:**This is the region of the bath tub curve where the failure rate is relatively *low* and *constant*. BFR estimations address this portion of the semiconductor component's lifecycle. This failure rate is quantified in units of Failure In Time (FIT) – which is an estimate of the number of failures that can occur in a billion (10^9) cumulative hours of the product's operation.
- **Intrinsic wear-out:** This is a period of the product's lifecycle when intrinsic wear-out dominates and failures increase exponentially. The end of a product's useful lifetime is specified as the time of onset of wear-out. These types of failures are caused by well-known factors such as channel-hot-carrier effects, electromigration, time-dependent dielectric breakdown and negative bias temperature instability. Functional safety standards such as ISO 26262 and IEC 61508 do not support the calculation of random hardware metrics based on a nonconstant fail rate. Consequently, a constant (but pessimistic) approximation over a product's lifetime is used to estimate BFR.

The system integrator has to contend with random hardware faults during normal useful life as well as the onset of wear-out. In such circumstances, system integrators must rely on safety mechanisms, which provide a certain diagnostic coverage and lower the risk (which is determined by severity, exposure, and controllability) to an acceptable value.

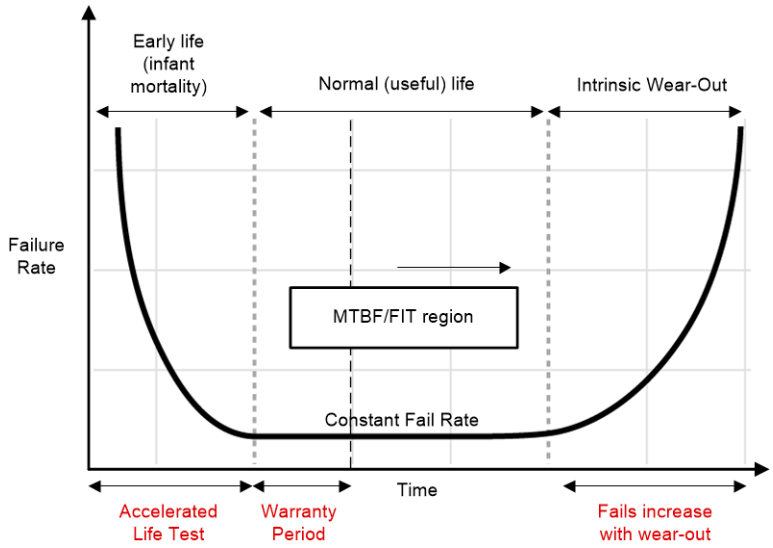


Figure 3-1. The Bathtub Curve is a Classic Representation of Random Hardware Faults

4 BFR Estimation Techniques

Various techniques exist for estimating BFR: experimental, derived from field observations of incidents and customer returns/field failures, or an estimation based on industry-accepted reliability guides coupled with some engineering judgment.

Here are a few examples of empirical techniques; however, these only account for intrinsic (silicon) failures and disregard the contribution from silicon and package interactions:

- Temperature bias operating life test
- High-temperature operating life test
- Extended life reliability test

Field observations, conversely, require accurate and extensive record keeping, and this is not available when a new product is introduced to market. Additionally, many semiconductor manufacturers do not receive all of the customer returns, making it impossible to meet the requirement for accurate and extensive records to estimate BFR.

The following industry reliability guides can provide a estimation for functional safety analysis:

- IEC technical report (TR) 62380 [3] and IEC 61709 [5]
- SN 29500, the Siemens AG standard for the reliability prediction of electronic and electromechanical components
- FIDES such as a military handbook or other documentation from a credible source

The remainder of this paper focuses on the use of IEC TR 62380 and SN 29500 to estimate BFR.

5 Siemens SN 29500 FIT model

SN 29500 uses a look-up table to find reference FIT rate and temperature for various component types such as:

- Integrated circuits (ICs)
- Discrete semiconductors
- Passive components
- Switches, relays, lamps, connectors, and so on

The method for estimating the FIT rate of an IC starts by looking up a reference FIT rate value and reference die temperature value from tables. The tables are separated into three types: one table for integrated circuits, a second one for discrete semiconductors and a third one for passive components. These three tables are further divided into subcategories of IC/component type and then by a range of how many transistors are in the IC or discrete semiconductor component.

In the excerpt shown in Figure 5-1, which is from a TI functional safety FIT document for a bipolar operational amplifier, the λ_{ref} FIT rate is 12 FIT and the reference die temperature is 55°C. This information is sourced from the SN 29500 standard.

FIT Siemens Norm SN29500 (2)			
Table	Category	Ref FIT λ_{ref}	Ref Virtual Tj $\theta_{vj,1}$
4	Bipolar Op Amp	12 FIT	55 C

Figure 5-1. TI Standard Functional Safety FIT Documentation for the SN 29500 Standard

The SN 29500 standard includes calculations for adjusting the FIT rate from the reference condition to the FIT rate for the actual expected system operating conditions. Simply plug in the expected temperature profile and reference values into the equations, and calculate the component's FIT rate in the context of the component's use in the intended application.

The following expresses the general equation for all types of components as:

Application FIT rate = reference FIT rate and temperature × temperature factors × voltage factors × current factors × % time stress factors

System integrators need to refer to the information in the SN 29500 standard to derive the specific FIT rate of the application for a TI-supplied component.

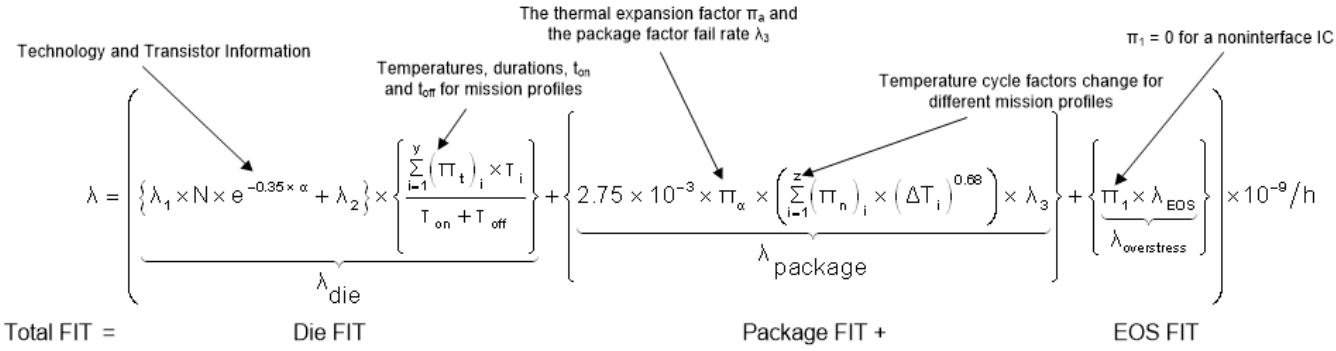
6 IEC TR 62380

The IEC 62380 standard is also commonly used when estimating BFR in functional safety analysis. It is a reliability data handbook that outlines a universal model for predicting the reliability of electronic components, printed circuit boards (PCBs) and equipment. It was published in 2004, and subsequently obsoleted. However, the ISO 26262 standard (now in second edition, revised in 2018) has incorporated the IEC 62380 standard as part of the newly published *Part 11 – Guidelines on Application of ISO 26262 to Semiconductors*.

The IEC TR 62380 IC failure rate can be modeled as sum of the die, package and electrical overstress (EOS) related failure rates, where:

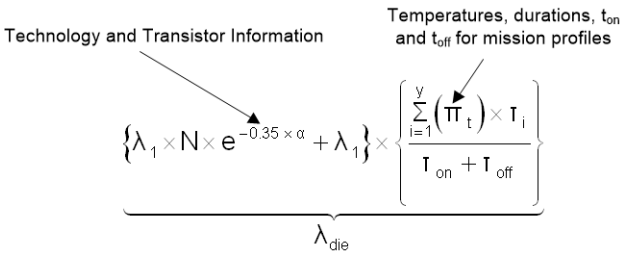
- The die-related failure rate formula includes terms for IC type and IC technology, transistor count, thermal mission profile, junction temperature, and operating and non-operating lifetime.
- The package-related failure rate formula includes terms for mechanical stress caused by thermal expansions, thermal cycles, thermal mission profile, package type and package materials.
- The EOS failure rate formula includes terms for specific systems with an external interface and electrical environment.

Equation 1 shows the IEC TR 62380 BFR formula (reproduced from the original standard). System integrators must refer to the IEC 62380 standard to access the information required to calculate BFR.



(1)

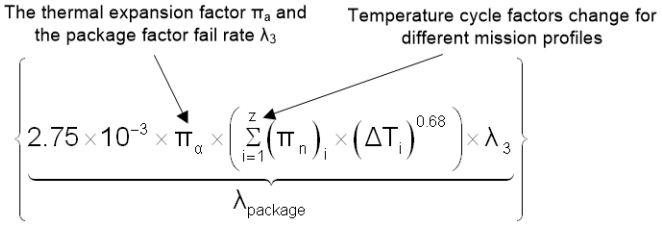
Equation 2 expresses the die FIT according to IEC TR 62380 as:



(2)

- where *N* is the number transistor by type, λ_1 is the transistor type scale factor, λ_2 is the technology base fit rate and α is a factor for the current year of manufacture.

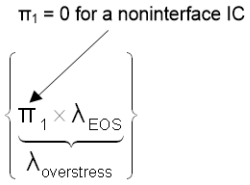
Equation 3 expresses the package FIT according to IEC TR 62380:



(3)

- where π_α is the difference in thermal expansion coefficients of the IC vs. the PCB and λ_3 is the package scale factor by package type and size.

Equation 4 expresses the EOS FIT according to IEC TR 62380:



(4)

- where the default assumption is that EOS = 0.

If the IC application is listed in the table and the system has an external connection between the IC on the circuit board and the outside environment, then system integrators can add EOS values as needed.

Table 6-1 reflects data from a table for an automotive mission profile according to IEC TR 62380. According to this table, the overall working time for an automotive motor control application is approximately 500 hours per year with four day time starts, two night time starts, and 30-days a year of non-use.

Table 6-1. Mission Profiles for Representative Applications from IEC TR 62380

Mission Profile Phases	Temp. 1		Temp 2.		Temp. 3		Ratios on/off		2 Night Starts		4 Day Light Starts		Non-Used Vehicle	
Application Types	$(t_{ac})1$ °c	t_1	$(t_{ac})2$ °c	t_2	$(t_{ac})3$ °c	t_3	t_{on}	t_{off}	n1 Cycles/ year	ΔT_1 °C/ cycle	n_2 Cycles/ year	ΔT_2 °C/ cycle	n_2 Cycles/ year	ΔT_3 °C/ cycle
Motor Control	32	0.020	60	0.015	85	0.023	0.058	0.942	670	$\frac{\Delta Tj}{3} + 55$	1340	$\frac{\Delta Tj}{3} + 45$	30	10
Passenger Compartment	27	0.006	30	0.046	85	0.006	0.058	0.942	670	$\frac{\Delta Tj}{3} + 30$	1340	$\frac{\Delta Tj}{3} + 20$	30	10

7 Recommended Assumptions for BFR Calculations

- Choose only one technique and use that technique consistently. The technique can be any of the following:
  - Empirical
  - Based on field data
    - State the model (Weibull or exponential) used for failure rate derived from field data
  - Based on reliability guide. (TI products use BFRs derived from reliability guides.)
- Assume a usage profile. Here are a couple of examples:
  - Industrial: always on 24/7 year-round until a scheduled preventive maintenance cycle
  - Automotive motor control: two to four starts per day, approximately 4 hours per day of use, as in IEC TR 62380
- Select (and state) the confidence interval (75%, 80%, 90%) for the underlying statistics used in the estimation
- Clearly document any scaling factors or derates that have gone into the BFR estimation
- Account for non-operating time and solder-joint-based failures

As long as all semiconductor suppliers use the same BFR estimation assumptions – or at minimum explicitly state the assumptions – it is possible to compare the BFRs of comparable semiconductor components from two different manufacturers.

8 Special Considerations for Transient Faults

Soft errors that result from a radiation event (internal or external) that can cause random hardware failures must be accounted for in a BFR estimate. However, do not include soft errors caused by electromagnetic interference or crosstalk in BFR calculations because these are classified as systematic faults, which are manageable by adhering to good design practices. It is possible to modulate transient faults through attributes such as:

- The technology used
- The impact of the fault and when applicable
- Standard versus low alpha versus ultra-low alpha mold compounds in packages

Architectural Vulnerability Factor (AVF) is the probability that a fault in a design structure, due to a soft error, results in a visible error in the final output of the function. According to ISO 26262, do not de-rate the BFR for soft errors based on AVF or safety mechanisms such as error detection and correction (EDAC) circuitry. Thus, it is best to calculate the BFR for soft errors separately for random access memory versus logic blocks in semiconductor components.

9 BFR Differences (Due to Package) Between IEC TR 62380 and SN 29500

SN 29500 is deficient (vs. IEC TR 62380) in accounting for failures that are due to silicon and package interactions. Consequently, functional safety standards recommend that:

- Semiconductor component manufacturers estimate failures caused by silicon interaction with package materials and silicon-to-package connection points (pins)
- System integrators account for failures attributable to the connection points between the semiconductor component and the boards (solder joints). These failures are typically analyzed at the *element* or *system* level.
- ISO 26262 defines:
  - An element as a system, components (hardware or software), hardware parts, or software units; and
  - A system as a set of components or subsystems that relates at least a sensor, a controller and an actuator with one another.

IEC TR 62380 accounts for both the interaction between silicon die and the lead frame/substrate and the connection between solder joints. In contrast, the package failure rate in SN 29500 only considers die-to-package interactions, which leads to inherent optimism in BFR estimations when using SN 29500.

10 Effect of Power-on Hours on BFR

ISO 26262 recommends applying these attributes to minimize the scaling or unjustifiable reduction of the calculated BFR:

- An accurate mission profile
- Assessing the applicability of failure modes in the operating conditions (as specified in the mission profile)
- Determining the fail rate per unit (on the per-hour, day, month or year for which the system is operated)

The BFR formula in IEC TR 62380 accounts for τ_{ON} and τ_{OFF}, whereas SN 29500 accounts for τ_{W}.

11 What Can You Expect for TI Products

TI has three categories of functional safety products: Functional Safety-Compliant, Functional Safety Quality-Managed and Functional Safety-Capable. More information on TI's functional safety products are available here. All TI functional safety products promoted for applicability in functionally safe systems come with functional safety FIT rate and failure mode distribution (FMD).

For our most complex products like microprocessors, microcontrollers and analog signal-chain products, system integrators get a comprehensive failure modes, effects and diagnostics analysis (FMEDA) that is inclusive of the FMD based on a BFR estimated according to IEC TR 62380.

For our least complex analog products, like low dropout oscillators, operational amplifiers and voltage supervisors, system integrators receive a functional safety FIT, pin failure mode analysis and a FMD report that adhere to a standard TI-wide format.

Links to example reports that outline this information follow:

- Texas Instruments, Functional Safety FIT Rate, Failure Mode Distribution TPS7A16A-Q1
- Texas Instruments, Functional Safety FIT Rate, Failure Mode Distribution TPS3851-Q1

12 Summary

System integrators can create safer, reliable designs faster with products, engineering expertise, and design resources from TI. Additionally, system integrators can meet the rigorous requirements of functional safety standards, such as ISO 26262 and IEC 61508, by choosing products that come with a BFR based on either IEC TR 62380 or SN 29500.

13 References

1. IEC 61508: Second edition 2010-04: Functional safety of electrical/electronic/programmable electronic safety – related systems.
2. ISO 26262: Second Edition 2018-12: Road Vehicles – Functional Safety, ISO 26262, International Organization for Standardization (2018)
3. IEC/TR 62380:2004(E): Reliability data handbook – Universal model for reliability prediction of electronics components, PCBs and equipment
4. SN 29500: Siemens Norm SN 29500/ Edition 2010-09
5. IEC 61709: Third Edition 2017-02: Electric components – Reliability – Reference conditions for failure rates and stress models for conversion

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (December 2023)	Page
• Changed SIL 2 PFH value from ≤100 FIT to ≤1000 FIT in Table 2-2	2

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